DATA SHEET

(DOC No. HX8238-A-DS)

HX8238-A

960 x 240 TFT LCD Single Chip Digital Driver

Preliminary version 01 November, 2006

Himax Technologies, Inc.
http://www.himax.com.tw

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List of Contents

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List of Figures

1. General Description

HX8238-A is a single chip controller and driver LSI that integrated the power circuit. It can drive a maximum 960x240 dot graphics on a-TFT panel displays in 262K colors. HX8238-A has a low-voltage operation, 1.4 min. In addition, HX8238-A is equipped with a DC-DC converter control circuit that generates the supply voltage for source and gate drivers with minimum external components. A common voltage generation circuit is included to drive the TFT-display counter electrode. An integrated gamma control circuit is also included that can be adjusted by software commands to provide maximum flexibility and optimal display quality.
HX8238-A is suitable for any medium-sized or small portable battery-driven product requiring long-term driving capabilities, such as Digital Still Cameras.

2. Features

- 960 x 240 graphics display a-TFT panel controller/driver for 262K colors.
- Support digital 8-bits serial/24-bits parallel RGB and CCIR601/656 input mode.
- Power supply:
  VDD = 1.8V – 2.50V (non-regulated input for logic)
  VDDIO = 1.4V – 3.60V (regulated input for logic)
  VCI = 2.50V – 3.60V (power supply for internal analog circuit)
- Maximum gate driving output voltage: 30Vp-p
- Source driving output voltage: 0-5V
- Low current sleep mode and 8-color display mode for power saving.
- Display size: 960 x 240.
- Support N-line inversion.
- Support Contrast/Brightness control
- Source and gate scan direction control.
- On-chip voltage generator.
- On-chip DC-DC converter up to 6x / -6x.
- Programmable gamma correction curve.
- Non-Volatile Memory (OTP) for VCOM calibration
- Programmable common electrode voltage amplitude and level for Cs on common structure only
- PWM function to generate power for backlight control
- COG package

3. Block Diagram

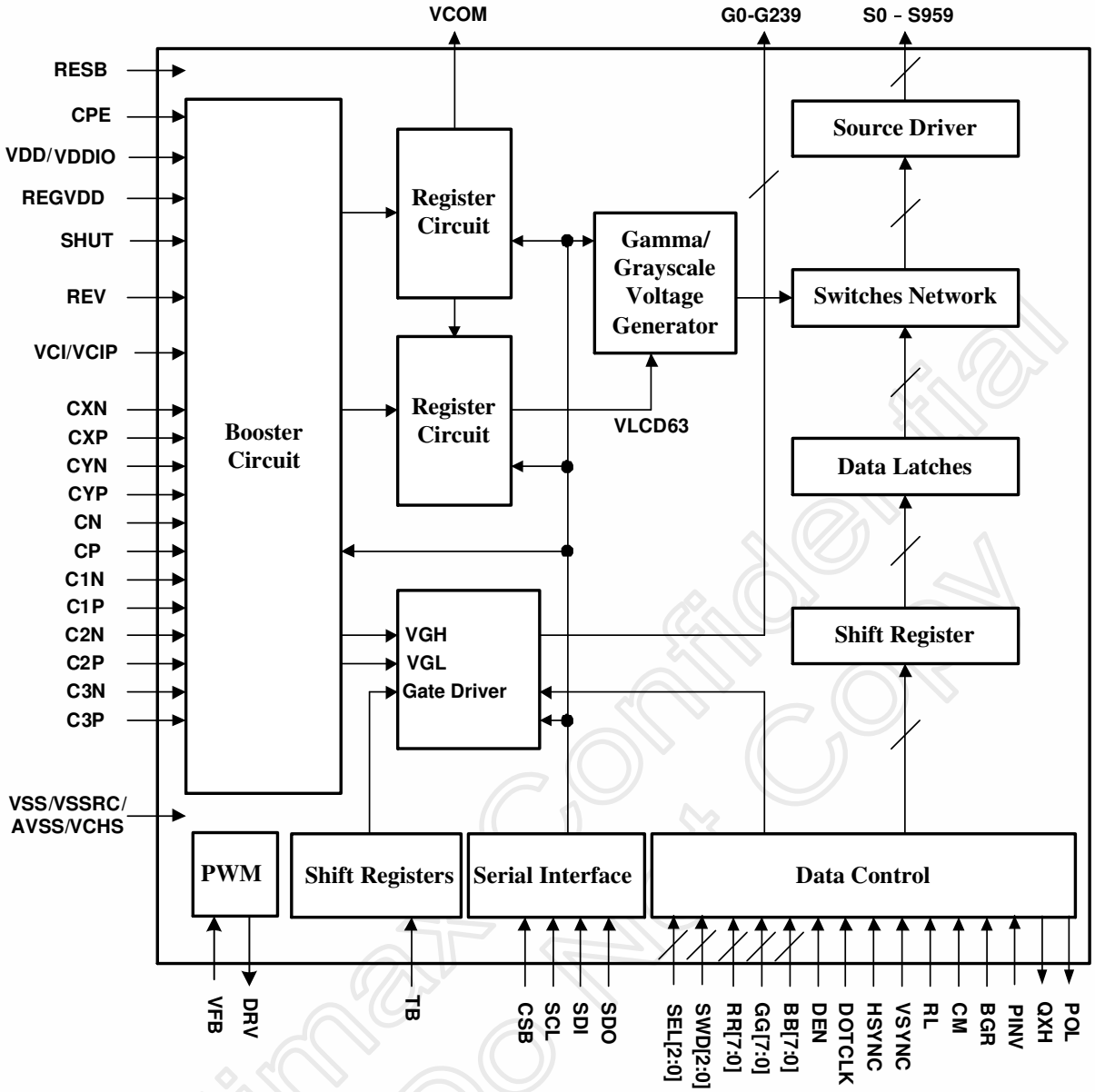
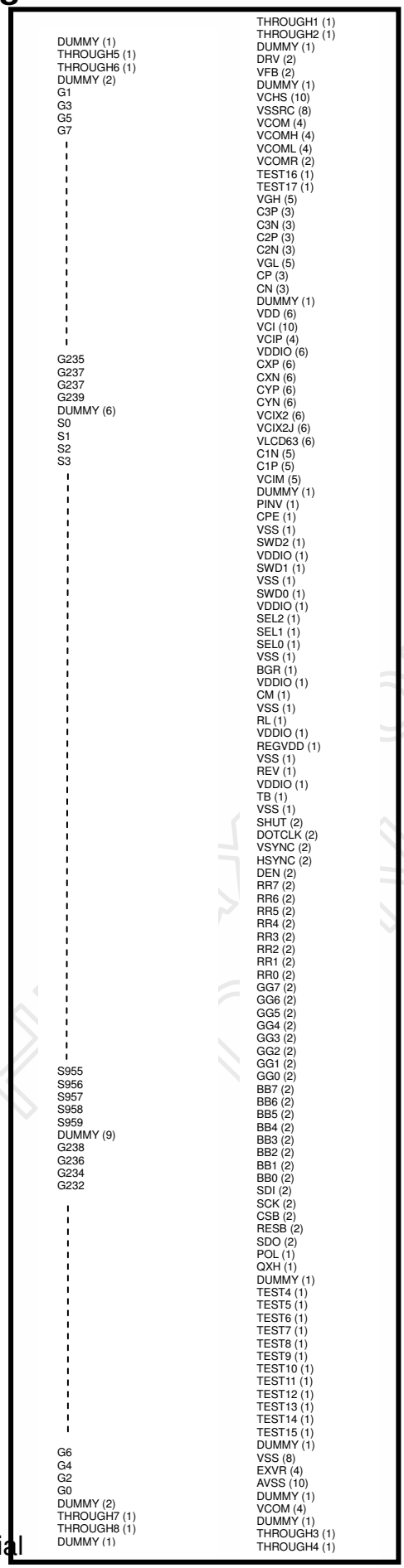
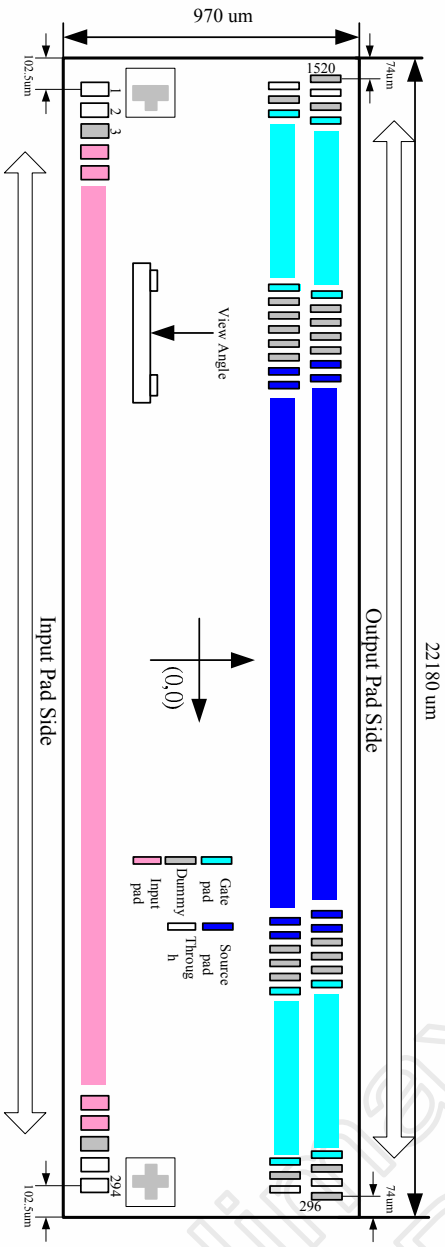
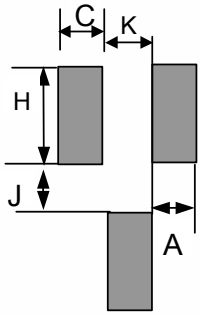


Figure 3. 1 HX8238-A block diagram description

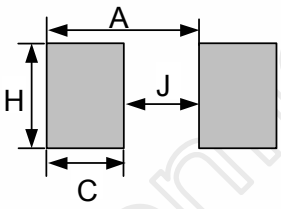
4. PAD Assignment





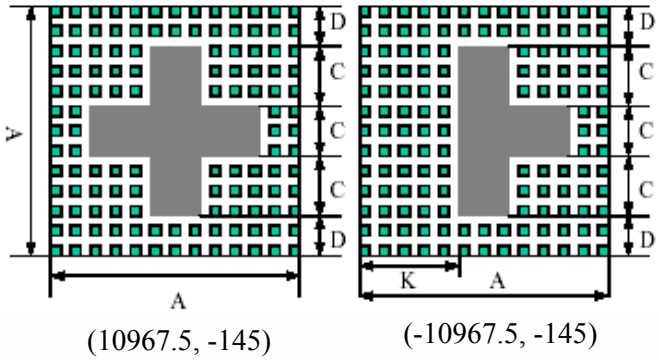


Output Pad	symbol	Size
Bump pitch	A	18um
Bump width	C	18um
Bump height	H	100um
Bump gap1 (Vertical)	J	30um
Bump gap2 (Horizontal)	K	18um
Bump area	C x H	1800um^2



Input Pad	symbol	Size
Bump pitch	A	75um
Bump width	C	50um
Bump height	H	110um
Bump gap1 (Vertical)	J	25um
Bump area	C x H	5500um2

Alignment Mark	symbol	Size
Alignment mark size	A	105um
Clearance gap 1	D	15um
Clearance gap 2	K	40um
Alignment mark width	C	25um
Alignment area	A x A	11025um^2



Die Size approximately: 22180 x 970 um^2
Bump Height: 15 um +/- 3um
Bump Hardness: 60 Hv +/- 15 Hv

Figure 4. 1 HX8238-A die floor plan (bump face up)

5. PAD Coordinate

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
1	THROUGH4	-10987.5	-365	50x110
2	THROUGH3	-10912.5	-365	50x110
3	DUMMY	-10837.5	-365	50x110
4	VCOM	-10762.5	-365	50x110
5	VCOM	-10687.5	-365	50x110
6	VCOM	-10612.5	-365	50x110
7	VCOM	-10537.5	-365	50x110
8	DUMMY	-10462.5	-365	50x110
9	AVSS	-10387.5	-365	50x110
10	AVSS	-10312.5	-365	50x110
11	AVSS	-10237.5	-365	50x110
12	AVSS	-10162.5	-365	50x110
13	AVSS	-10087.5	-365	50x110
14	AVSS	-10012.5	-365	50x110
15	AVSS	-9937.5	-365	50x110
16	AVSS	-9862.5	-365	50x110
17	AVSS	-9787.5	-365	50x110
18	AVSS	-9712.5	-365	50x110
19	EXVR	-9637.5	-365	50x110
20	EXVR	-9562.5	-365	50x110
21	EXVR	-9487.5	-365	50x110
22	EXVR	-9412.5	-365	50x110
23	VSS	-9337.5	-365	50x110
24	VSS	-9262.5	-365	50x110
25	VSS	-9187.5	-365	50x110
26	VSS	-9112.5	-365	50x110
27	VSS	-9037.5	-365	50x110
28	VSS	-8962.5	-365	50x110
29	VSS	-8887.5	-365	50x110
30	VSS	-8812.5	-365	50x110
31	DUMMY	-8737.5	-365	50x110
32	TEST15	-8662.5	-365	50x110
33	TEST14	-8587.5	-365	50x110
34	TEST13	-8512.5	-365	50x110
35	TEST12	-8437.5	-365	50x110
36	TEST11	-8362.5	-365	50x110
37	TEST10	-8287.5	-365	50x110
38	TEST9	-8212.5	-365	50x110
39	TEST8	-8137.5	-365	50x110
40	TEST7	-8062.5	-365	50x110
41	TEST6	-7987.5	-365	50x110
42	TEST5	-7912.5	-365	50x110
43	TEST4	-7837.5	-365	50x110
44	DUMMY	-7762.5	-365	50x110
45	QXH	-7687.5	-365	50x110
46	POL	-7612.5	-365	50x110
47	SDO	-7537.5	-365	50x110
48	SDO	-7462.5	-365	50x110
49	RESB	-7387.5	-365	50x110
50	RESB	-7312.5	-365	50x110

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
51	CSB	-7237.5	-365	50x110
52	CSB	-7162.5	-365	50x110
53	SCK	-7087.5	-365	50x110
54	SCK	-7012.5	-365	50x110
55	SDI	-6937.5	-365	50x110
56	SDI	-6862.5	-365	50x110
57	BB0	-6787.5	-365	50x110
58	BB0	-6712.5	-365	50x110
59	BB1	-6637.5	-365	50x110
60	BB1	-6562.5	-365	50x110
61	BB2	-6487.5	-365	50x110
62	BB2	-6412.5	-365	50x110
63	BB3	-6337.5	-365	50x110
64	BB3	-6262.5	-365	50x110
65	BB4	-6187.5	-365	50x110
66	BB4	-6112.5	-365	50x110
67	BB5	-6037.5	-365	50x110
68	BB5	-5962.5	-365	50x110
69	BB6	-5887.5	-365	50x110
70	BB6	-5812.5	-365	50x110
71	BB7	-5737.5	-365	50x110
72	BB7	-5662.5	-365	50x110
73	GG0	-5587.5	-365	50x110
74	GG0	-5512.5	-365	50x110
75	GG1	-5437.5	-365	50x110
76	GG1	-5362.5	-365	50x110
77	GG2	-5287.5	-365	50x110
78	GG2	-5212.5	-365	50x110
79	GG3	-5137.5	-365	50x110
80	GG3	-5062.5	-365	50x110
81	GG4	-4987.5	-365	50x110
82	GG4	-4912.5	-365	50x110
83	GG5	-4837.5	-365	50x110
84	GG5	-4762.5	-365	50x110
85	GG6	-4687.5	-365	50x110
86	GG6	-4612.5	-365	50x110
87	GG7	-4537.5	-365	50x110
88	GG7	-4462.5	-365	50x110
89	RR0	-4387.5	-365	50x110
90	RR0	-4312.5	-365	50x110
91	RR1	-4237.5	-365	50x110
92	RR1	-4162.5	-365	50x110
93	RR2	-4087.5	-365	50x110
94	RR2	-4012.5	-365	50x110
95	RR3	-3937.5	-365	50x110
96	RR3	-3862.5	-365	50x110
97	RR4	-3787.5	-365	50x110
98	RR4	-3712.5	-365	50x110
99	RR5	-3637.5	-365	50x110
100	RR5	-3562.5	-365	50x110

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
101	RR6	-3487.5	-365	50x110
102	RR6	-3412.5	-365	50x110
103	RR7	-3337.5	-365	50x110
104	RR7	-3262.5	-365	50x110
105	DEN	-3187.5	-365	50x110
106	DEN	-3112.5	-365	50x110
107	HSYNC	-3037.5	-365	50x110
108	HSYNC	-2962.5	-365	50x110
109	VSYNC	-2887.5	-365	50x110
110	VSYNC	-2812.5	-365	50x110
111	DOTCLK	-2737.5	-365	50x110
112	DOTCLK	-2662.5	-365	50x110
113	SHUT	-2587.5	-365	50x110
114	SHUT	-2512.5	-365	50x110
115	VSS	-2437.5	-365	50x110
116	TB	-2362.5	-365	50x110
117	VDDIO	-2287.5	-365	50x110
118	REV	-2212.5	-365	50x110
119	VSS	-2137.5	-365	50x110
120	REGVDD	-2062.5	-365	50x110
121	VDDIO	-1987.5	-365	50x110
122	RL	-1912.5	-365	50x110
123	VSS	-1837.5	-365	50x110
124	CM	-1762.5	-365	50x110
125	VDDIO	-1687.5	-365	50x110
126	BGR	-1612.5	-365	50x110
127	VSS	-1537.5	-365	50x110
128	SEL0	-1462.5	-365	50x110
129	SEL1	-1387.5	-365	50x110
130	SEL2	-1312.5	-365	50x110
131	VDDIO	-1237.5	-365	50x110
132	SWD0	-1162.5	-365	50x110
133	VSS	-1087.5	-365	50x110
134	SWD1	-1012.5	-365	50x110
135	VDDIO	-937.5	-365	50x110
136	SWD2	-862.5	-365	50x110
137	VSS	-787.5	-365	50x110
138	CPE	-712.5	-365	50x110
139	PINV	-637.5	-365	50x110
140	DUMMY	-562.5	-365	50x110
141	VCIM	-487.5	-365	50x110
142	VCIM	-412.5	-365	50x110
143	VCIM	-337.5	-365	50x110
144	VCIM	-262.5	-365	50x110
145	VCIM	-187.5	-365	50x110
146	C1P	-112.5	-365	50x110
147	C1P	-37.5	-365	50x110
148	C1P	37.5	-365	50x110
149	C1P	112.5	-365	50x110
150	C1P	187.5	-365	50x110

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
151	C1N	262.5	-365	50x110
152	C1N	337.5	-365	50x110
153	C1N	412.5	-365	50x110
154	C1N	487.5	-365	50x110
155	C1N	562.5	-365	50x110
156	VLCD63	637.5	-365	50x110
157	VLCD63	712.5	-365	50x110
158	VLCD63	787.5	-365	50x110
159	VLCD63	862.5	-365	50x110
160	VLCD63	937.5	-365	50x110
161	VLCD63	1012.5	-365	50x110
162	VCIX2J	1087.5	-365	50x110
163	VCIX2J	1162.5	-365	50x110
164	VCIX2J	1237.5	-365	50x110
165	VCIX2J	1312.5	-365	50x110
166	VCIX2J	1387.5	-365	50x110
167	VCIX2J	1462.5	-365	50x110
168	VCIX2	1537.5	-365	50x110
169	VCIX2	1612.5	-365	50x110
170	VCIX2	1687.5	-365	50x110
171	VCIX2	1762.5	-365	50x110
172	VCIX2	1837.5	-365	50x110
173	VCIX2	1912.5	-365	50x110
174	CYN	1987.5	-365	50x110
175	CYN	2062.5	-365	50x110
176	CYN	2137.5	-365	50x110
177	CYN	2212.5	-365	50x110
178	CYN	2287.5	-365	50x110
179	CYN	2362.5	-365	50x110
180	CYP	2437.5	-365	50x110
181	CYP	2512.5	-365	50x110
182	CYP	2587.5	-365	50x110
183	CYP	2662.5	-365	50x110
184	CYP	2737.5	-365	50x110
185	CYP	2812.5	-365	50x110
186	CXN	2887.5	-365	50x110
187	CXN	2962.5	-365	50x110
188	CXN	3037.5	-365	50x110
189	CXN	3112.5	-365	50x110
190	CXN	3187.5	-365	50x110
191	CXN	3262.5	-365	50x110
192	CXP	3337.5	-365	50x110
193	CXP	3412.5	-365	50x110
194	CXP	3487.5	-365	50x110
195	CXP	3562.5	-365	50x110
196	CXP	3637.5	-365	50x110
197	CXP	3712.5	-365	50x110
198	VDDIO	3787.5	-365	50x110
199	VDDIO	3862.5	-365	50x110
200	VDDIO	3937.5	-365	50x110

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
201	VDDIO	4012.5	-365	50x110
202	VDDIO	4087.5	-365	50x110
203	VDDIO	4162.5	-365	50x110
204	VCIP	4237.5	-365	50x110
205	VCIP	4312.5	-365	50x110
206	VCIP	4387.5	-365	50x110
207	VCIP	4462.5	-365	50x110
208	VCI	4537.5	-365	50x110
209	VCI	4612.5	-365	50x110
210	VCI	4687.5	-365	50x110
211	VCI	4762.5	-365	50x110
212	VCI	4837.5	-365	50x110
213	VCI	4912.5	-365	50x110
214	VCI	4987.5	-365	50x110
215	VCI	5062.5	-365	50x110
216	VCI	5137.5	-365	50x110
217	VCI	5212.5	-365	50x110
218	VDD	5287.5	-365	50x110
219	VDD	5362.5	-365	50x110
220	VDD	5437.5	-365	50x110
221	VDD	5512.5	-365	50x110
222	VDD	5587.5	-365	50x110
223	VDD	5662.5	-365	50x110
224	DUMMY	5737.5	-365	50x110
225	CN	5812.5	-365	50x110
226	CN	5887.5	-365	50x110
227	CN	5962.5	-365	50x110
228	CP	6037.5	-365	50x110
229	CP	6112.5	-365	50x110
230	CP	6187.5	-365	50x110
231	VGL	6262.5	-365	50x110
232	VGL	6337.5	-365	50x110
233	VGL	6412.5	-365	50x110
234	VGL	6487.5	-365	50x110
235	VGL	6562.5	-365	50x110
236	C2N	6637.5	-365	50x110
237	C2N	6712.5	-365	50x110
238	C2N	6787.5	-365	50x110
239	C2P	6862.5	-365	50x110
240	C2P	6937.5	-365	50x110
241	C2P	7012.5	-365	50x110
242	C3N	7087.5	-365	50x110
243	C3N	7162.5	-365	50x110
244	C3N	7237.5	-365	50x110
245	C3P	7312.5	-365	50x110
246	C3P	7387.5	-365	50x110
247	C3P	7462.5	-365	50x110
248	VGH	7537.5	-365	50x110
249	VGH	7612.5	-365	50x110
250	VGH	7687.5	-365	50x110

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
251	VGH	7762.5	-365	50x110
252	VGH	7837.5	-365	50x110
253	TEST17	7912.5	-365	50x110
254	TEST16	7987.5	-365	50x110
255	VCOMR	8062.5	-365	50x110
256	VCOMR	8137.5	-365	50x110
257	VCOML	8212.5	-365	50x110
258	VCOML	8287.5	-365	50x110
259	VCOML	8362.5	-365	50x110
260	VCOML	8437.5	-365	50x110
261	VCOMH	8512.5	-365	50x110
262	VCOMH	8587.5	-365	50x110
263	VCOMH	8662.5	-365	50x110
264	VCOMH	8737.5	-365	50x110
265	VCOM	8812.5	-365	50x110
266	VCOM	8887.5	-365	50x110
267	VCOM	8962.5	-365	50x110
268	VCOM	9037.5	-365	50x110
269	VSSRC	9112.5	-365	50x110
270	VSSRC	9187.5	-365	50x110
271	VSSRC	9262.5	-365	50x110
272	VSSRC	9337.5	-365	50x110
273	VSSRC	9412.5	-365	50x110
274	VSSRC	9487.5	-365	50x110
275	VSSRC	9562.5	-365	50x110
276	VSSRC	9637.5	-365	50x110
277	VCHS	9712.5	-365	50x110
278	VCHS	9787.5	-365	50x110
279	VCHS	9862.5	-365	50x110
280	VCHS	9937.5	-365	50x110
281	VCHS	10012.5	-365	50x110
282	VCHS	10087.5	-365	50x110
283	VCHS	10162.5	-365	50x110
284	VCHS	10237.5	-365	50x110
285	VCHS	10312.5	-365	50x110
286	VCHS	10387.5	-365	50x110
287	DUMMY	10462.5	-365	50x110
288	VFB	10537.5	-365	50x110
289	VFB	10612.5	-365	50x110
290	DRV	10687.5	-365	50x110
291	DRV	10762.5	-365	50x110
292	DUMMY	10837.5	-365	50x110
293	THROUGH2	10912.5	-365	50x110
294	THROUGH1	10987.5	-365	50x110
295	R_MARK	10967.5	-145	NA
296	DUMMY	11016	370	18x100
297	THROUGH5	10998	240	18x100
298	THROUGH6	10980	370	18x100
299	DUMMY	10962	240	18x100
300	DUMMY	10944	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
301	G1	10926	240	18x100
302	G3	10908	370	18x100
303	G5	10890	240	18x100
304	G7	10872	370	18x100
305	G9	10854	240	18x100
306	G11	10836	370	18x100
307	G13	10818	240	18x100
308	G15	10800	370	18x100
309	G17	10782	240	18x100
310	G19	10764	370	18x100
311	G21	10746	240	18x100
312	G23	10728	370	18x100
313	G25	10710	240	18x100
314	G27	10692	370	18x100
315	G29	10674	240	18x100
316	G31	10656	370	18x100
317	G33	10638	240	18x100
318	G35	10620	370	18x100
319	G37	10602	240	18x100
320	G39	10584	370	18x100
321	G41	10566	240	18x100
322	G43	10548	370	18x100
323	G45	10530	240	18x100
324	G47	10512	370	18x100
325	G49	10494	240	18x100
326	G51	10476	370	18x100
327	G53	10458	240	18x100
328	G55	10440	370	18x100
329	G57	10422	240	18x100
330	G59	10404	370	18x100
331	G61	10386	240	18x100
332	G63	10368	370	18x100
333	G65	10350	240	18x100
334	G67	10332	370	18x100
335	G69	10314	240	18x100
336	G71	10296	370	18x100
337	G73	10278	240	18x100
338	G75	10260	370	18x100
339	G77	10242	240	18x100
340	G79	10224	370	18x100
341	G81	10206	240	18x100
342	G83	10188	370	18x100
343	G85	10170	240	18x100
344	G87	10152	370	18x100
345	G89	10134	240	18x100
346	G91	10116	370	18x100
347	G93	10098	240	18x100
348	G95	10080	370	18x100
349	G97	10062	240	18x100
350	G99	10044	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
351	G101	10026	240	18x100
352	G103	10008	370	18x100
353	G105	9990	240	18x100
354	G107	9972	370	18x100
355	G109	9954	240	18x100
356	G111	9936	370	18x100
357	G113	9918	240	18x100
358	G115	9900	370	18x100
359	G117	9882	240	18x100
360	G119	9864	370	18x100
361	G121	9846	240	18x100
362	G123	9828	370	18x100
363	G125	9810	240	18x100
364	G127	9792	370	18x100
365	G129	9774	240	18x100
366	G131	9756	370	18x100
367	G133	9738	240	18x100
368	G135	9720	370	18x100
369	G137	9702	240	18x100
370	G139	9684	370	18x100
371	G141	9666	240	18x100
372	G143	9648	370	18x100
373	G145	9630	240	18x100
374	G147	9612	370	18x100
375	G149	9594	240	18x100
376	G151	9576	370	18x100
377	G153	9558	240	18x100
378	G155	9540	370	18x100
379	G157	9522	240	18x100
380	G159	9504	370	18x100
381	G161	9486	240	18x100
382	G163	9468	370	18x100
383	G165	9450	240	18x100
384	G167	9432	370	18x100
385	G169	9414	240	18x100
386	G171	9396	370	18x100
387	G173	9378	240	18x100
388	G175	9360	370	18x100
389	G177	9342	240	18x100
390	G179	9324	370	18x100
391	G181	9306	240	18x100
392	G183	9288	370	18x100
393	G185	9270	240	18x100
394	G187	9252	370	18x100
395	G189	9234	240	18x100
396	G191	9216	370	18x100
397	G193	9198	240	18x100
398	G195	9180	370	18x100
399	G197	9162	240	18x100
400	G199	9144	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
401	G201	9126	240	18x100
402	G203	9108	370	18x100
403	G205	9090	240	18x100
404	G207	9072	370	18x100
405	G209	9054	240	18x100
406	G211	9036	370	18x100
407	G213	9018	240	18x100
408	G215	9000	370	18x100
409	G217	8982	240	18x100
410	G219	8964	370	18x100
411	G221	8946	240	18x100
412	G223	8928	370	18x100
413	G225	8910	240	18x100
414	G227	8892	370	18x100
415	G229	8874	240	18x100
416	G231	8856	370	18x100
417	G233	8838	240	18x100
418	G235	8820	370	18x100
419	G237	8802	240	18x100
420	G239	8784	370	18x100
421	DUMMY	8766	240	18x100
422	DUMMY	8748	370	18x100
423	DUMMY	8730	240	18x100
424	DUMMY	8712	370	18x100
425	DUMMY	8694	240	18x100
426	DUMMY	8676	370	18x100
427	S0	8658	240	18x100
428	S1	8640	370	18x100
429	S2	8622	240	18x100
430	S3	8604	370	18x100
431	S4	8586	240	18x100
432	S5	8568	370	18x100
433	S6	8550	240	18x100
434	S7	8532	370	18x100
435	S8	8514	240	18x100
436	S9	8496	370	18x100
437	S10	8478	240	18x100
438	S11	8460	370	18x100
439	S12	8442	240	18x100
440	S13	8424	370	18x100
441	S14	8406	240	18x100
442	S15	8388	370	18x100
443	S16	8370	240	18x100
444	S17	8352	370	18x100
445	S18	8334	240	18x100
446	S19	8316	370	18x100
447	S20	8298	240	18x100
448	S21	8280	370	18x100
449	S22	8262	240	18x100
450	S23	8244	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
451	S24	8226	240	18x100
452	S25	8208	370	18x100
453	S26	8190	240	18x100
454	S27	8172	370	18x100
455	S28	8154	240	18x100
456	S29	8136	370	18x100
457	S30	8118	240	18x100
458	S31	8100	370	18x100
459	S32	8082	240	18x100
460	S33	8064	370	18x100
461	S34	8046	240	18x100
462	S35	8028	370	18x100
463	S36	8010	240	18x100
464	S37	7992	370	18x100
465	S38	7974	240	18x100
466	S39	7956	370	18x100
467	S40	7938	240	18x100
468	S41	7920	370	18x100
469	S42	7902	240	18x100
470	S43	7884	370	18x100
471	S44	7866	240	18x100
472	S45	7848	370	18x100
473	S46	7830	240	18x100
474	S47	7812	370	18x100
475	S48	7794	240	18x100
476	S49	7776	370	18x100
477	S50	7758	240	18x100
478	S51	7740	370	18x100
479	S52	7722	240	18x100
480	S53	7704	370	18x100
481	S54	7686	240	18x100
482	S55	7668	370	18x100
483	S56	7650	240	18x100
484	S57	7632	370	18x100
485	S58	7614	240	18x100
486	S59	7596	370	18x100
487	S60	7578	240	18x100
488	S61	7560	370	18x100
489	S62	7542	240	18x100
490	S63	7524	370	18x100
491	S64	7506	240	18x100
492	S65	7488	370	18x100
493	S66	7470	240	18x100
494	S67	7452	370	18x100
495	S68	7434	240	18x100
496	S69	7416	370	18x100
497	S70	7398	240	18x100
498	S71	7380	370	18x100
499	S72	7362	240	18x100
500	S73	7344	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
501	S74	7326	240	18x100
502	S75	7308	370	18x100
503	S76	7290	240	18x100
504	S77	7272	370	18x100
505	S78	7254	240	18x100
506	S79	7236	370	18x100
507	S80	7218	240	18x100
508	S81	7200	370	18x100
509	S82	7182	240	18x100
510	S83	7164	370	18x100
511	S84	7146	240	18x100
512	S85	7128	370	18x100
513	S86	7110	240	18x100
514	S87	7092	370	18x100
515	S88	7074	240	18x100
516	S89	7056	370	18x100
517	S90	7038	240	18x100
518	S91	7020	370	18x100
519	S92	7002	240	18x100
520	S93	6984	370	18x100
521	S94	6966	240	18x100
522	S95	6948	370	18x100
523	S96	6930	240	18x100
524	S97	6912	370	18x100
525	S98	6894	240	18x100
526	S99	6876	370	18x100
527	S100	6858	240	18x100
528	S101	6840	370	18x100
529	S102	6822	240	18x100
530	S103	6804	370	18x100
531	S104	6786	240	18x100
532	S105	6768	370	18x100
533	S106	6750	240	18x100
534	S107	6732	370	18x100
535	S108	6714	240	18x100
536	S109	6696	370	18x100
537	S110	6678	240	18x100
538	S111	6660	370	18x100
539	S112	6642	240	18x100
540	S113	6624	370	18x100
541	S114	6606	240	18x100
542	S115	6588	370	18x100
543	S116	6570	240	18x100
544	S117	6552	370	18x100
545	S118	6534	240	18x100
546	S119	6516	370	18x100
547	S120	6498	240	18x100
548	S121	6480	370	18x100
549	S122	6462	240	18x100
550	S123	6444	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
551	S124	6426	240	18x100
552	S125	6408	370	18x100
553	S126	6390	240	18x100
554	S127	6372	370	18x100
555	S128	6354	240	18x100
556	S129	6336	370	18x100
557	S130	6318	240	18x100
558	S131	6300	370	18x100
559	S132	6282	240	18x100
560	S133	6264	370	18x100
561	S134	6246	240	18x100
562	S135	6228	370	18x100
563	S136	6210	240	18x100
564	S137	6192	370	18x100
565	S138	6174	240	18x100
566	S139	6156	370	18x100
567	S140	6138	240	18x100
568	S141	6120	370	18x100
569	S142	6102	240	18x100
570	S143	6084	370	18x100
571	S144	6066	240	18x100
572	S145	6048	370	18x100
573	S146	6030	240	18x100
574	S147	6012	370	18x100
575	S148	5994	240	18x100
576	S149	5976	370	18x100
577	S150	5958	240	18x100
578	S151	5940	370	18x100
579	S152	5922	240	18x100
580	S153	5904	370	18x100
581	S154	5886	240	18x100
582	S155	5868	370	18x100
583	S156	5850	240	18x100
584	S157	5832	370	18x100
585	S158	5814	240	18x100
586	S159	5796	370	18x100
587	S160	5778	240	18x100
588	S161	5760	370	18x100
589	S162	5742	240	18x100
590	S163	5724	370	18x100
591	S164	5706	240	18x100
592	S165	5688	370	18x100
593	S166	5670	240	18x100
594	S167	5652	370	18x100
595	S168	5634	240	18x100
596	S169	5616	370	18x100
597	S170	5598	240	18x100
598	S171	5580	370	18x100
599	S172	5562	240	18x100
600	S173	5544	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
601	S174	5526	240	18x100
602	S175	5508	370	18x100
603	S176	5490	240	18x100
604	S177	5472	370	18x100
605	S178	5454	240	18x100
606	S179	5436	370	18x100
607	S180	5418	240	18x100
608	S181	5400	370	18x100
609	S182	5382	240	18x100
610	S183	5364	370	18x100
611	S184	5346	240	18x100
612	S185	5328	370	18x100
613	S186	5310	240	18x100
614	S187	5292	370	18x100
615	S188	5274	240	18x100
616	S189	5256	370	18x100
617	S190	5238	240	18x100
618	S191	5220	370	18x100
619	S192	5202	240	18x100
620	S193	5184	370	18x100
621	S194	5166	240	18x100
622	S195	5148	370	18x100
623	S196	5130	240	18x100
624	S197	5112	370	18x100
625	S198	5094	240	18x100
626	S199	5076	370	18x100
627	S200	5058	240	18x100
628	S201	5040	370	18x100
629	S202	5022	240	18x100
630	S203	5004	370	18x100
631	S204	4986	240	18x100
632	S205	4968	370	18x100
633	S206	4950	240	18x100
634	S207	4932	370	18x100
635	S208	4914	240	18x100
636	S209	4896	370	18x100
637	S210	4878	240	18x100
638	S211	4860	370	18x100
639	S212	4842	240	18x100
640	S213	4824	370	18x100
641	S214	4806	240	18x100
642	S215	4788	370	18x100
643	S216	4770	240	18x100
644	S217	4752	370	18x100
645	S218	4734	240	18x100
646	S219	4716	370	18x100
647	S220	4698	240	18x100
648	S221	4680	370	18x100
649	S222	4662	240	18x100
650	S223	4644	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
651	S224	4626	240	18x100
652	S225	4608	370	18x100
653	S226	4590	240	18x100
654	S227	4572	370	18x100
655	S228	4554	240	18x100
656	S229	4536	370	18x100
657	S230	4518	240	18x100
658	S231	4500	370	18x100
659	S232	4482	240	18x100
660	S233	4464	370	18x100
661	S234	4446	240	18x100
662	S235	4428	370	18x100
663	S236	4410	240	18x100
664	S237	4392	370	18x100
665	S238	4374	240	18x100
666	S239	4356	370	18x100
667	S240	4338	240	18x100
668	S241	4320	370	18x100
669	S242	4302	240	18x100
670	S243	4284	370	18x100
671	S244	4266	240	18x100
672	S245	4248	370	18x100
673	S246	4230	240	18x100
674	S247	4212	370	18x100
675	S248	4194	240	18x100
676	S249	4176	370	18x100
677	S250	4158	240	18x100
678	S251	4140	370	18x100
679	S252	4122	240	18x100
680	S253	4104	370	18x100
681	S254	4086	240	18x100
682	S255	4068	370	18x100
683	S256	4050	240	18x100
684	S257	4032	370	18x100
685	S258	4014	240	18x100
686	S259	3996	370	18x100
687	S260	3978	240	18x100
688	S261	3960	370	18x100
689	S262	3942	240	18x100
690	S263	3924	370	18x100
691	S264	3906	240	18x100
692	S265	3888	370	18x100
693	S266	3870	240	18x100
694	S267	3852	370	18x100
695	S268	3834	240	18x100
696	S269	3816	370	18x100
697	S270	3798	240	18x100
698	S271	3780	370	18x100
699	S272	3762	240	18x100
700	S273	3744	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
701	S274	3726	240	18x100
702	S275	3708	370	18x100
703	S276	3690	240	18x100
704	S277	3672	370	18x100
705	S278	3654	240	18x100
706	S279	3636	370	18x100
707	S280	3618	240	18x100
708	S281	3600	370	18x100
709	S282	3582	240	18x100
710	S283	3564	370	18x100
711	S284	3546	240	18x100
712	S285	3528	370	18x100
713	S286	3510	240	18x100
714	S287	3492	370	18x100
715	S288	3474	240	18x100
716	S289	3456	370	18x100
717	S290	3438	240	18x100
718	S291	3420	370	18x100
719	S292	3402	240	18x100
720	S293	3384	370	18x100
721	S294	3366	240	18x100
722	S295	3348	370	18x100
723	S296	3330	240	18x100
724	S297	3312	370	18x100
725	S298	3294	240	18x100
726	S299	3276	370	18x100
727	S300	3258	240	18x100
728	S301	3240	370	18x100
729	S302	3222	240	18x100
730	S303	3204	370	18x100
731	S304	3186	240	18x100
732	S305	3168	370	18x100
733	S306	3150	240	18x100
734	S307	3132	370	18x100
735	S308	3114	240	18x100
736	S309	3096	370	18x100
737	S310	3078	240	18x100
738	S311	3060	370	18x100
739	S312	3042	240	18x100
740	S313	3024	370	18x100
741	S314	3006	240	18x100
742	S315	2988	370	18x100
743	S316	2970	240	18x100
744	S317	2952	370	18x100
745	S318	2934	240	18x100
746	S319	2916	370	18x100
747	S320	2898	240	18x100
748	S321	2880	370	18x100
749	S322	2862	240	18x100
750	S323	2844	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
751	S324	2826	240	18x100
752	S325	2808	370	18x100
753	S326	2790	240	18x100
754	S327	2772	370	18x100
755	S328	2754	240	18x100
756	S329	2736	370	18x100
757	S330	2718	240	18x100
758	S331	2700	370	18x100
759	S332	2682	240	18x100
760	S333	2664	370	18x100
761	S334	2646	240	18x100
762	S335	2628	370	18x100
763	S336	2610	240	18x100
764	S337	2592	370	18x100
765	S338	2574	240	18x100
766	S339	2556	370	18x100
767	S340	2538	240	18x100
768	S341	2520	370	18x100
769	S342	2502	240	18x100
770	S343	2484	370	18x100
771	S344	2466	240	18x100
772	S345	2448	370	18x100
773	S346	2430	240	18x100
774	S347	2412	370	18x100
775	S348	2394	240	18x100
776	S349	2376	370	18x100
777	S350	2358	240	18x100
778	S351	2340	370	18x100
779	S352	2322	240	18x100
780	S353	2304	370	18x100
781	S354	2286	240	18x100
782	S355	2268	370	18x100
783	S356	2250	240	18x100
784	S357	2232	370	18x100
785	S358	2214	240	18x100
786	S359	2196	370	18x100
787	S360	2178	240	18x100
788	S361	2160	370	18x100
789	S362	2142	240	18x100
790	S363	2124	370	18x100
791	S364	2106	240	18x100
792	S365	2088	370	18x100
793	S366	2070	240	18x100
794	S367	2052	370	18x100
795	S368	2034	240	18x100
796	S369	2016	370	18x100
797	S370	1998	240	18x100
798	S371	1980	370	18x100
799	S372	1962	240	18x100
800	S373	1944	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
801	S374	1926	240	18x100
802	S375	1908	370	18x100
803	S376	1890	240	18x100
804	S377	1872	370	18x100
805	S378	1854	240	18x100
806	S379	1836	370	18x100
807	S380	1818	240	18x100
808	S381	1800	370	18x100
809	S382	1782	240	18x100
810	S383	1764	370	18x100
811	S384	1746	240	18x100
812	S385	1728	370	18x100
813	S386	1710	240	18x100
814	S387	1692	370	18x100
815	S388	1674	240	18x100
816	S389	1656	370	18x100
817	S390	1638	240	18x100
818	S391	1620	370	18x100
819	S392	1602	240	18x100
820	S393	1584	370	18x100
821	S394	1566	240	18x100
822	S395	1548	370	18x100
823	S396	1530	240	18x100
824	S397	1512	370	18x100
825	S398	1494	240	18x100
826	S399	1476	370	18x100
827	S400	1458	240	18x100
828	S401	1440	370	18x100
829	S402	1422	240	18x100
830	S403	1404	370	18x100
831	S404	1386	240	18x100
832	S405	1368	370	18x100
833	S406	1350	240	18x100
834	S407	1332	370	18x100
835	S408	1314	240	18x100
836	S409	1296	370	18x100
837	S410	1278	240	18x100
838	S411	1260	370	18x100
839	S412	1242	240	18x100
840	S413	1224	370	18x100
841	S414	1206	240	18x100
842	S415	1188	370	18x100
843	S416	1170	240	18x100
844	S417	1152	370	18x100
845	S418	1134	240	18x100
846	S419	1116	370	18x100
847	S420	1098	240	18x100
848	S421	1080	370	18x100
849	S422	1062	240	18x100
850	S423	1044	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
851	S424	1026	240	18x100
852	S425	1008	370	18x100
853	S426	990	240	18x100
854	S427	972	370	18x100
855	S428	954	240	18x100
856	S429	936	370	18x100
857	S430	918	240	18x100
858	S431	900	370	18x100
859	S432	882	240	18x100
860	S433	864	370	18x100
861	S434	846	240	18x100
862	S435	828	370	18x100
863	S436	810	240	18x100
864	S437	792	370	18x100
865	S438	774	240	18x100
866	S439	756	370	18x100
867	S440	738	240	18x100
868	S441	720	370	18x100
869	S442	702	240	18x100
870	S443	684	370	18x100
871	S444	666	240	18x100
872	S445	648	370	18x100
873	S446	630	240	18x100
874	S447	612	370	18x100
875	S448	594	240	18x100
876	S449	576	370	18x100
877	S450	558	240	18x100
878	S451	540	370	18x100
879	S452	522	240	18x100
880	S453	504	370	18x100
881	S454	486	240	18x100
882	S455	468	370	18x100
883	S456	450	240	18x100
884	S457	432	370	18x100
885	S458	414	240	18x100
886	S459	396	370	18x100
887	S460	378	240	18x100
888	S461	360	370	18x100
889	S462	342	240	18x100
890	S463	324	370	18x100
891	S464	306	240	18x100
892	S465	288	370	18x100
893	S466	270	240	18x100
894	S467	252	370	18x100
895	S468	234	240	18x100
896	S469	216	370	18x100
897	S470	198	240	18x100
898	S471	180	370	18x100
899	S472	162	240	18x100
900	S473	144	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
901	S474	126	240	18x100
902	S475	108	370	18x100
903	S476	90	240	18x100
904	S477	72	370	18x100
905	S478	54	240	18x100
906	S479	36	370	18x100
907	S480	18	240	18x100
908	S481	0	370	18x100
909	S482	-18	240	18x100
910	S483	-36	370	18x100
911	S484	-54	240	18x100
912	S485	-72	370	18x100
913	S486	-90	240	18x100
914	S487	-108	370	18x100
915	S488	-126	240	18x100
916	S489	-144	370	18x100
917	S490	-162	240	18x100
918	S491	-180	370	18x100
919	S492	-198	240	18x100
920	S493	-216	370	18x100
921	S494	-234	240	18x100
922	S495	-252	370	18x100
923	S496	-270	240	18x100
924	S497	-288	370	18x100
925	S498	-306	240	18x100
926	S499	-324	370	18x100
927	S500	-342	240	18x100
928	S501	-360	370	18x100
929	S502	-378	240	18x100
930	S503	-396	370	18x100
931	S504	-414	240	18x100
932	S505	-432	370	18x100
933	S506	-450	240	18x100
934	S507	-468	370	18x100
935	S508	-486	240	18x100
936	S509	-504	370	18x100
937	S510	-522	240	18x100
938	S511	-540	370	18x100
939	S512	-558	240	18x100
940	S513	-576	370	18x100
941	S514	-594	240	18x100
942	S515	-612	370	18x100
943	S516	-630	240	18x100
944	S517	-648	370	18x100
945	S518	-666	240	18x100
946	S519	-684	370	18x100
947	S520	-702	240	18x100
948	S521	-720	370	18x100
949	S522	-738	240	18x100
950	S523	-756	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
951	S524	-774	240	18x100
952	S525	-792	370	18x100
953	S526	-810	240	18x100
954	S527	-828	370	18x100
955	S528	-846	240	18x100
956	S529	-864	370	18x100
957	S530	-882	240	18x100
958	S531	-900	370	18x100
959	S532	-918	240	18x100
960	S533	-936	370	18x100
961	S534	-954	240	18x100
962	S535	-972	370	18x100
963	S536	-990	240	18x100
964	S537	-1008	370	18x100
965	S538	-1026	240	18x100
966	S539	-1044	370	18x100
967	S540	-1062	240	18x100
968	S541	-1080	370	18x100
969	S542	-1098	240	18x100
970	S543	-1116	370	18x100
971	S544	-1134	240	18x100
972	S545	-1152	370	18x100
973	S546	-1170	240	18x100
974	S547	-1188	370	18x100
975	S548	-1206	240	18x100
976	S549	-1224	370	18x100
977	S550	-1242	240	18x100
978	S551	-1260	370	18x100
979	S552	-1278	240	18x100
980	S553	-1296	370	18x100
981	S554	-1314	240	18x100
982	S555	-1332	370	18x100
983	S556	-1350	240	18x100
984	S557	-1368	370	18x100
985	S558	-1386	240	18x100
986	S559	-1404	370	18x100
987	S560	-1422	240	18x100
988	S561	-1440	370	18x100
989	S562	-1458	240	18x100
990	S563	-1476	370	18x100
991	S564	-1494	240	18x100
992	S565	-1512	370	18x100
993	S566	-1530	240	18x100
994	S567	-1548	370	18x100
995	S568	-1566	240	18x100
996	S569	-1584	370	18x100
997	S570	-1602	240	18x100
998	S571	-1620	370	18x100
999	S572	-1638	240	18x100
1000	S573	-1656	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
1001	S574	-1674	240	18x100
1002	S575	-1692	370	18x100
1003	S576	-1710	240	18x100
1004	S577	-1728	370	18x100
1005	S578	-1746	240	18x100
1006	S579	-1764	370	18x100
1007	S580	-1782	240	18x100
1008	S581	-1800	370	18x100
1009	S582	-1818	240	18x100
1010	S583	-1836	370	18x100
1011	S584	-1854	240	18x100
1012	S585	-1872	370	18x100
1013	S586	-1890	240	18x100
1014	S587	-1908	370	18x100
1015	S588	-1926	240	18x100
1016	S589	-1944	370	18x100
1017	S590	-1962	240	18x100
1018	S591	-1980	370	18x100
1019	S592	-1998	240	18x100
1020	S593	-2016	370	18x100
1021	S594	-2034	240	18x100
1022	S595	-2052	370	18x100
1023	S596	-2070	240	18x100
1024	S597	-2088	370	18x100
1025	S598	-2106	240	18x100
1026	S599	-2124	370	18x100
1027	S600	-2142	240	18x100
1028	S601	-2160	370	18x100
1029	S602	-2178	240	18x100
1030	S603	-2196	370	18x100
1031	S604	-2214	240	18x100
1032	S605	-2232	370	18x100
1033	S606	-2250	240	18x100
1034	S607	-2268	370	18x100
1035	S608	-2286	240	18x100
1036	S609	-2304	370	18x100
1037	S610	-2322	240	18x100
1038	S611	-2340	370	18x100
1039	S612	-2358	240	18x100
1040	S613	-2376	370	18x100
1041	S614	-2394	240	18x100
1042	S615	-2412	370	18x100
1043	S616	-2430	240	18x100
1044	S617	-2448	370	18x100
1045	S618	-2466	240	18x100
1046	S619	-2484	370	18x100
1047	S620	-2502	240	18x100
1048	S621	-2520	370	18x100
1049	S622	-2538	240	18x100
1050	S623	-2556	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
1051	S624	-2574	240	18x100
1052	S625	-2592	370	18x100
1053	S626	-2610	240	18x100
1054	S627	-2628	370	18x100
1055	S628	-2646	240	18x100
1056	S629	-2664	370	18x100
1057	S630	-2682	240	18x100
1058	S631	-2700	370	18x100
1059	S632	-2718	240	18x100
1060	S633	-2736	370	18x100
1061	S634	-2754	240	18x100
1062	S635	-2772	370	18x100
1063	S636	-2790	240	18x100
1064	S637	-2808	370	18x100
1065	S638	-2826	240	18x100
1066	S639	-2844	370	18x100
1067	S640	-2862	240	18x100
1068	S641	-2880	370	18x100
1069	S642	-2898	240	18x100
1070	S643	-2916	370	18x100
1071	S644	-2934	240	18x100
1072	S645	-2952	370	18x100
1073	S646	-2970	240	18x100
1074	S647	-2988	370	18x100
1075	S648	-3006	240	18x100
1076	S649	-3024	370	18x100
1077	S650	-3042	240	18x100
1078	S651	-3060	370	18x100
1079	S652	-3078	240	18x100
1080	S653	-3096	370	18x100
1081	S654	-3114	240	18x100
1082	S655	-3132	370	18x100
1083	S656	-3150	240	18x100
1084	S657	-3168	370	18x100
1085	S658	-3186	240	18x100
1086	S659	-3204	370	18x100
1087	S660	-3222	240	18x100
1088	S661	-3240	370	18x100
1089	S662	-3258	240	18x100
1090	S663	-3276	370	18x100
1091	S664	-3294	240	18x100
1092	S665	-3312	370	18x100
1093	S666	-3330	240	18x100
1094	S667	-3348	370	18x100
1095	S668	-3366	240	18x100
1096	S669	-3384	370	18x100
1097	S670	-3402	240	18x100
1098	S671	-3420	370	18x100
1099	S672	-3438	240	18x100
1100	S673	-3456	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
1101	S674	-3474	240	18x100
1102	S675	-3492	370	18x100
1103	S676	-3510	240	18x100
1104	S677	-3528	370	18x100
1105	S678	-3546	240	18x100
1106	S679	-3564	370	18x100
1107	S680	-3582	240	18x100
1108	S681	-3600	370	18x100
1109	S682	-3618	240	18x100
1110	S683	-3636	370	18x100
1111	S684	-3654	240	18x100
1112	S685	-3672	370	18x100
1113	S686	-3690	240	18x100
1114	S687	-3708	370	18x100
1115	S688	-3726	240	18x100
1116	S689	-3744	370	18x100
1117	S690	-3762	240	18x100
1118	S691	-3780	370	18x100
1119	S692	-3798	240	18x100
1120	S693	-3816	370	18x100
1121	S694	-3834	240	18x100
1122	S695	-3852	370	18x100
1123	S696	-3870	240	18x100
1124	S697	-3888	370	18x100
1125	S698	-3906	240	18x100
1126	S699	-3924	370	18x100
1127	S700	-3942	240	18x100
1128	S701	-3960	370	18x100
1129	S702	-3978	240	18x100
1130	S703	-3996	370	18x100
1131	S704	-4014	240	18x100
1132	S705	-4032	370	18x100
1133	S706	-4050	240	18x100
1134	S707	-4068	370	18x100
1135	S708	-4086	240	18x100
1136	S709	-4104	370	18x100
1137	S710	-4122	240	18x100
1138	S711	-4140	370	18x100
1139	S712	-4158	240	18x100
1140	S713	-4176	370	18x100
1141	S714	-4194	240	18x100
1142	S715	-4212	370	18x100
1143	S716	-4230	240	18x100
1144	S717	-4248	370	18x100
1145	S718	-4266	240	18x100
1146	S719	-4284	370	18x100
1147	S720	-4302	240	18x100
1148	S721	-4320	370	18x100
1149	S722	-4338	240	18x100
1150	S723	-4356	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
1151	S724	-4374	240	18x100
1152	S725	-4392	370	18x100
1153	S726	-4410	240	18x100
1154	S727	-4428	370	18x100
1155	S728	-4446	240	18x100
1156	S729	-4464	370	18x100
1157	S730	-4482	240	18x100
1158	S731	-4500	370	18x100
1159	S732	-4518	240	18x100
1160	S733	-4536	370	18x100
1161	S734	-4554	240	18x100
1162	S735	-4572	370	18x100
1163	S736	-4590	240	18x100
1164	S737	-4608	370	18x100
1165	S738	-4626	240	18x100
1166	S739	-4644	370	18x100
1167	S740	-4662	240	18x100
1168	S741	-4680	370	18x100
1169	S742	-4698	240	18x100
1170	S743	-4716	370	18x100
1171	S744	-4734	240	18x100
1172	S745	-4752	370	18x100
1173	S746	-4770	240	18x100
1174	S747	-4788	370	18x100
1175	S748	-4806	240	18x100
1176	S749	-4824	370	18x100
1177	S750	-4842	240	18x100
1178	S751	-4860	370	18x100
1179	S752	-4878	240	18x100
1180	S753	-4896	370	18x100
1181	S754	-4914	240	18x100
1182	S755	-4932	370	18x100
1183	S756	-4950	240	18x100
1184	S757	-4968	370	18x100
1185	S758	-4986	240	18x100
1186	S759	-5004	370	18x100
1187	S760	-5022	240	18x100
1188	S761	-5040	370	18x100
1189	S762	-5058	240	18x100
1190	S763	-5076	370	18x100
1191	S764	-5094	240	18x100
1192	S765	-5112	370	18x100
1193	S766	-5130	240	18x100
1194	S767	-5148	370	18x100
1195	S768	-5166	240	18x100
1196	S769	-5184	370	18x100
1197	S770	-5202	240	18x100
1198	S771	-5220	370	18x100
1199	S772	-5238	240	18x100
1200	S773	-5256	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
1201	S774	-5274	240	18x100
1202	S775	-5292	370	18x100
1203	S776	-5310	240	18x100
1204	S777	-5328	370	18x100
1205	S778	-5346	240	18x100
1206	S779	-5364	370	18x100
1207	S780	-5382	240	18x100
1208	S781	-5400	370	18x100
1209	S782	-5418	240	18x100
1210	S783	-5436	370	18x100
1211	S784	-5454	240	18x100
1212	S785	-5472	370	18x100
1213	S786	-5490	240	18x100
1214	S787	-5508	370	18x100
1215	S788	-5526	240	18x100
1216	S789	-5544	370	18x100
1217	S790	-5562	240	18x100
1218	S791	-5580	370	18x100
1219	S792	-5598	240	18x100
1220	S793	-5616	370	18x100
1221	S794	-5634	240	18x100
1222	S795	-5652	370	18x100
1223	S796	-5670	240	18x100
1224	S797	-5688	370	18x100
1225	S798	-5706	240	18x100
1226	S799	-5724	370	18x100
1227	S800	-5742	240	18x100
1228	S801	-5760	370	18x100
1229	S802	-5778	240	18x100
1230	S803	-5796	370	18x100
1231	S804	-5814	240	18x100
1232	S805	-5832	370	18x100
1233	S806	-5850	240	18x100
1234	S807	-5868	370	18x100
1235	S808	-5886	240	18x100
1236	S809	-5904	370	18x100
1237	S810	-5922	240	18x100
1238	S811	-5940	370	18x100
1239	S812	-5958	240	18x100
1240	S813	-5976	370	18x100
1241	S814	-5994	240	18x100
1242	S815	-6012	370	18x100
1243	S816	-6030	240	18x100
1244	S817	-6048	370	18x100
1245	S818	-6066	240	18x100
1246	S819	-6084	370	18x100
1247	S820	-6102	240	18x100
1248	S821	-6120	370	18x100
1249	S822	-6138	240	18x100
1250	S823	-6156	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
1251	S824	-6174	240	18x100
1252	S825	-6192	370	18x100
1253	S826	-6210	240	18x100
1254	S827	-6228	370	18x100
1255	S828	-6246	240	18x100
1256	S829	-6264	370	18x100
1257	S830	-6282	240	18x100
1258	S831	-6300	370	18x100
1259	S832	-6318	240	18x100
1260	S833	-6336	370	18x100
1261	S834	-6354	240	18x100
1262	S835	-6372	370	18x100
1263	S836	-6390	240	18x100
1264	S837	-6408	370	18x100
1265	S838	-6426	240	18x100
1266	S839	-6444	370	18x100
1267	S840	-6462	240	18x100
1268	S841	-6480	370	18x100
1269	S842	-6498	240	18x100
1270	S843	-6516	370	18x100
1271	S844	-6534	240	18x100
1272	S845	-6552	370	18x100
1273	S846	-6570	240	18x100
1274	S847	-6588	370	18x100
1275	S848	-6606	240	18x100
1276	S849	-6624	370	18x100
1277	S850	-6642	240	18x100
1278	S851	-6660	370	18x100
1279	S852	-6678	240	18x100
1280	S853	-6696	370	18x100
1281	S854	-6714	240	18x100
1282	S855	-6732	370	18x100
1283	S856	-6750	240	18x100
1284	S857	-6768	370	18x100
1285	S858	-6786	240	18x100
1286	S859	-6804	370	18x100
1287	S860	-6822	240	18x100
1288	S861	-6840	370	18x100
1289	S862	-6858	240	18x100
1290	S863	-6876	370	18x100
1291	S864	-6894	240	18x100
1292	S865	-6912	370	18x100
1293	S866	-6930	240	18x100
1294	S867	-6948	370	18x100
1295	S868	-6966	240	18x100
1296	S869	-6984	370	18x100
1297	S870	-7002	240	18x100
1298	S871	-7020	370	18x100
1299	S872	-7038	240	18x100
1300	S873	-7056	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
1301	S874	-7074	240	18x100
1302	S875	-7092	370	18x100
1303	S876	-7110	240	18x100
1304	S877	-7128	370	18x100
1305	S878	-7146	240	18x100
1306	S879	-7164	370	18x100
1307	S880	-7182	240	18x100
1308	S881	-7200	370	18x100
1309	S882	-7218	240	18x100
1310	S883	-7236	370	18x100
1311	S884	-7254	240	18x100
1312	S885	-7272	370	18x100
1313	S886	-7290	240	18x100
1314	S887	-7308	370	18x100
1315	S888	-7326	240	18x100
1316	S889	-7344	370	18x100
1317	S890	-7362	240	18x100
1318	S891	-7380	370	18x100
1319	S892	-7398	240	18x100
1320	S893	-7416	370	18x100
1321	S894	-7434	240	18x100
1322	S895	-7452	370	18x100
1323	S896	-7470	240	18x100
1324	S897	-7488	370	18x100
1325	S898	-7506	240	18x100
1326	S899	-7524	370	18x100
1327	S900	-7542	240	18x100
1328	S901	-7560	370	18x100
1329	S902	-7578	240	18x100
1330	S903	-7596	370	18x100
1331	S904	-7614	240	18x100
1332	S905	-7632	370	18x100
1333	S906	-7650	240	18x100
1334	S907	-7668	370	18x100
1335	S908	-7686	240	18x100
1336	S909	-7704	370	18x100
1337	S910	-7722	240	18x100
1338	S911	-7740	370	18x100
1339	S912	-7758	240	18x100
1340	S913	-7776	370	18x100
1341	S914	-7794	240	18x100
1342	S915	-7812	370	18x100
1343	S916	-7830	240	18x100
1344	S917	-7848	370	18x100
1345	S918	-7866	240	18x100
1346	S919	-7884	370	18x100
1347	S920	-7902	240	18x100
1348	S921	-7920	370	18x100
1349	S922	-7938	240	18x100
1350	S923	-7956	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
1351	S924	-7974	240	18x100
1352	S925	-7992	370	18x100
1353	S926	-8010	240	18x100
1354	S927	-8028	370	18x100
1355	S928	-8046	240	18x100
1356	S929	-8064	370	18x100
1357	S930	-8082	240	18x100
1358	S931	-8100	370	18x100
1359	S932	-8118	240	18x100
1360	S933	-8136	370	18x100
1361	S934	-8154	240	18x100
1362	S935	-8172	370	18x100
1363	S936	-8190	240	18x100
1364	S937	-8208	370	18x100
1365	S938	-8226	240	18x100
1366	S939	-8244	370	18x100
1367	S940	-8262	240	18x100
1368	S941	-8280	370	18x100
1369	S942	-8298	240	18x100
1370	S943	-8316	370	18x100
1371	S944	-8334	240	18x100
1372	S945	-8352	370	18x100
1373	S946	-8370	240	18x100
1374	S947	-8388	370	18x100
1375	S948	-8406	240	18x100
1376	S949	-8424	370	18x100
1377	S950	-8442	240	18x100
1378	S951	-8460	370	18x100
1379	S952	-8478	240	18x100
1380	S953	-8496	370	18x100
1381	S954	-8514	240	18x100
1382	S955	-8532	370	18x100
1383	S956	-8550	240	18x100
1384	S957	-8568	370	18x100
1385	S958	-8586	240	18x100
1386	S959	-8604	370	18x100
1387	DUMMY	-8622	240	18x100
1388	DUMMY	-8640	370	18x100
1389	DUMMY	-8658	240	18x100
1390	DUMMY	-8676	370	18x100
1391	DUMMY	-8694	240	18x100
1392	DUMMY	-8712	370	18x100
1393	DUMMY	-8730	240	18x100
1394	DUMMY	-8748	370	18x100
1395	DUMMY	-8766	240	18x100
1396	G238	-8784	370	18x100
1397	G236	-8802	240	18x100
1398	G234	-8820	370	18x100
1399	G232	-8838	240	18x100
1400	G230	-8856	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
1401	G228	-8874	240	18x100
1402	G226	-8892	370	18x100
1403	G224	-8910	240	18x100
1404	G222	-8928	370	18x100
1405	G220	-8946	240	18x100
1406	G218	-8964	370	18x100
1407	G216	-8982	240	18x100
1408	G214	-9000	370	18x100
1409	G212	-9018	240	18x100
1410	G210	-9036	370	18x100
1411	G208	-9054	240	18x100
1412	G206	-9072	370	18x100
1413	G204	-9090	240	18x100
1414	G202	-9108	370	18x100
1415	G200	-9126	240	18x100
1416	G198	-9144	370	18x100
1417	G196	-9162	240	18x100
1418	G194	-9180	370	18x100
1419	G192	-9198	240	18x100
1420	G190	-9216	370	18x100
1421	G188	-9234	240	18x100
1422	G186	-9252	370	18x100
1423	G184	-9270	240	18x100
1424	G182	-9288	370	18x100
1425	G180	-9306	240	18x100
1426	G178	-9324	370	18x100
1427	G176	-9342	240	18x100
1428	G174	-9360	370	18x100
1429	G172	-9378	240	18x100
1430	G170	-9396	370	18x100
1431	G168	-9414	240	18x100
1432	G166	-9432	370	18x100
1433	G164	-9450	240	18x100
1434	G162	-9468	370	18x100
1435	G160	-9486	240	18x100
1436	G158	-9504	370	18x100
1437	G156	-9522	240	18x100
1438	G154	-9540	370	18x100
1439	G152	-9558	240	18x100
1440	G150	-9576	370	18x100
1441	G148	-9594	240	18x100
1442	G146	-9612	370	18x100
1443	G144	-9630	240	18x100
1444	G142	-9648	370	18x100
1445	G140	-9666	240	18x100
1446	G138	-9684	370	18x100
1447	G136	-9702	240	18x100
1448	G134	-9720	370	18x100
1449	G132	-9738	240	18x100
1450	G130	-9756	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
1451	G128	-9774	240	18x100
1452	G126	-9792	370	18x100
1453	G124	-9810	240	18x100
1454	G122	-9828	370	18x100
1455	G120	-9846	240	18x100
1456	G118	-9864	370	18x100
1457	G116	-9882	240	18x100
1458	G114	-9900	370	18x100
1459	G112	-9918	240	18x100
1460	G110	-9936	370	18x100
1461	G108	-9954	240	18x100
1462	G106	-9972	370	18x100
1463	G104	-9990	240	18x100
1464	G102	-10008	370	18x100
1465	G100	-10026	240	18x100
1466	G98	-10044	370	18x100
1467	G96	-10062	240	18x100
1468	G94	-10080	370	18x100
1469	G92	-10098	240	18x100
1470	G90	-10116	370	18x100
1471	G88	-10134	240	18x100
1472	G86	-10152	370	18x100
1473	G84	-10170	240	18x100
1474	G82	-10188	370	18x100
1475	G80	-10206	240	18x100
1476	G78	-10224	370	18x100
1477	G76	-10242	240	18x100
1478	G74	-10260	370	18x100
1479	G72	-10278	240	18x100
1480	G70	-10296	370	18x100
1481	G68	-10314	240	18x100
1482	G66	-10332	370	18x100
1483	G64	-10350	240	18x100
1484	G62	-10368	370	18x100
1485	G60	-10386	240	18x100
1486	G58	-10404	370	18x100
1487	G56	-10422	240	18x100
1488	G54	-10440	370	18x100
1489	G52	-10458	240	18x100
1490	G50	-10476	370	18x100
1491	G48	-10494	240	18x100
1492	G46	-10512	370	18x100
1493	G44	-10530	240	18x100
1494	G42	-10548	370	18x100
1495	G40	-10566	240	18x100
1496	G38	-10584	370	18x100
1497	G36	-10602	240	18x100
1498	G34	-10620	370	18x100
1499	G32	-10638	240	18x100
1500	G30	-10656	370	18x100

PAD NO.	PAD NAME	X axis	Y axis	Bump Size
1501	G28	-10674	240	18x100
1502	G26	-10692	370	18x100
1503	G24	-10710	240	18x100
1504	G22	-10728	370	18x100
1505	G20	-10746	240	18x100
1506	G18	-10764	370	18x100
1507	G16	-10782	240	18x100
1508	G14	-10800	370	18x100
1509	G12	-10818	240	18x100
1510	G10	-10836	370	18x100
1511	G8	-10854	240	18x100
1512	G6	-10872	370	18x100
1513	G4	-10890	240	18x100
1514	G2	-10908	370	18x100
1515	G0	-10926	240	18x100
1516	DUMMY	-10944	370	18x100
1517	DUMMY	-10962	240	18x100
1518	THROUGH7	-10980	370	18x100
1519	THROUGH8	-10998	240	18x100
1520	DUMMY	-11016	370	18x100
1521	L_MARK	-10967.5	-145	NA

6. Pin Description

Name	I/O	Function	Description
CM	Input	Logic Control	Input pin to select 262k-color or 8-color display mode. After entered 8-color display mode, the driver will switch to Frame-Inversion-Mode, and only MSB of the data Red, Green and Blue will be considered. - Connect to VDDIO for 8-color display mode - Connect to VSS for 262k-color display mode
RR [7:0] GG [7:0] BB [7:0]	Input	Graphic Display Data	Graphic Data Input Pins. Internal pull low. - RR [7:0]: Red Data - 8-bits - GG [7:0]: Green Data - 8-bits - BB [7:0]: Blue Data - 8-bits For 8 bit interface, only RR[7:0] are used. For unused pins, please connect to VSS or floating.
DEN	Input	Display Timing Signals	Display enable pin from controller. Internal pull high. Connect to VDDIO or floating if not used.
VSYNC			Frame synchronization signal. Internal pull high. - Fixed to VDDIO or floating if not used.
HSYNC			Line synchronization signal. Internal pull high. - Fixed to VDDIO or floating if not used
DOTCLK			Dot-clock signal and oscillator source. A non-stop external clock must be provided to that pin even at front or black porch non-display period.
SHUT	Input	Logic Control	Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low. - Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode (Refer to Power Up Sequence)
RL	Input	Panel Mapping Control	Input pin to select the Source driver data shift direction. - Connect to VDDIO for display first RGB data at S0-S2 - Connect to VSS for display first RGB data at S959-S957
TB			Input pin to select the Gate driver scan direction. - Connect to VSS for Gate scan from G239 to G0 (reverse scan) - Connect to VDDIO for Gate scan from G0 to G239 (normal scan)
BGR			Input pin to select the color mapping. - Connect to VDDIO for Blue-Green-Red mapping - Connect to VSS for Red-Green-Blue mapping (See S0-S959 pin description for details)
REV			Input pin to select the display reversion. - Connect to VDDIO mapping data '0' to maximum pixel voltage for normally white panel - Connect to VSS for mapping data '0' to minimum pixel voltage for normally black panel
SWD[2:0]			Input pin to define color filter type. Reference register R04h.
SEL[2:0]			Input pin to select input interface mode. Reference register R04h. These pins are internal pull low.
CPE			Input pin to enable internal charge pump circuit. Internal pull high. - Connect to VDDIO to enable internal charge pump. - Connect to VSS to disable internal charge pump
QXH	Output		Data sequence control pin, this pin toggle each line under delta panel.
POL			Polarity signal to monitor VCOM signal
PINV	Input	POL Control	Control the polarity of POL signal. Internal pull low. - Connect to VDDIO, POL phase is reversed with internal VCOM signal - Connect to VSS, POL phase is same with internal VCOM signal
REGVDD	Input	Logic Control	Input pin to enable internal voltage regulation. -Connect to VDDIO if System Vdd > 2.5V or System Vdd < 1.8V -Connect to VSS if 2.5V ≥ System Vdd ≥ 1.8V, internal regulator will be disabled

Name	I/O	Function	Description
RESB	Input	System Reset	System reset pin. Internal pull high. - Connect to VDDIO when not used (Refer to Power Up Sequence)
CSB	Input	Serial Interface	Chip select pin of serial interface. Internal pull high. - Leave it OPEN when not used (Refer to Serial Interface block)
SCK			Clock pin of serial interface. Internal pull high. - Leave it OPEN when not used (Refer to Serial Interface block)
SDI			Data input pin in serial mode. Internal pull high. - Leave it OPEN when not used (Refer to Serial Interface block)
SDO	Output		Data output pin in serial mode. - Leave it OPEN when not used (Refer to Serial Interface block)
VDDIO	Power	Power Supply for Logic Circuits	Voltage input pin for I/O logic. - Connect to system Vdd
VDD			Voltage input pin for internal logic. a) REGVDD = VDDIO Internal regulator will be on for 3.6V ≥ System Vdd ≥ 2.5V or 1.6V ≥ System Vdd ≥ 1.4V, VDD ~2V. b) REGVDD = VSS Internal regulator will be off for 2.5V ≥ System Vdd ≥ 1.6V, VDD = System Vdd
VSS	Power	Ground of the Power Supply	System ground pin of the IC. - Connect to system ground
AVSS			Grounding for analog circuit. - Connect to system ground
VSSRC			Grounding for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages. - Connect to system ground.
VCHS			Grounding for booster circuit. - Connect to system ground.
VCI	Power	Power Supply for Analog Circuits	Booster input voltage pin. - Connect to voltage source between 2.5V to 3.6V
VCIP			Voltage supply pin for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages. - Connect to same source of VCI
VCIM	Output	Booster Voltages	Negative voltage of VCI. - Connect a capacitor for stabilization
VCIX2			Equals to 2 x VCI. - Connect a capacitor for stabilization
VCIX2J	Power	Voltage for Analog	This is the power supply used by on chip analog blocks and VGH/VGL dcdc.
EXVR	Input	External Reference	External reference of internal Gamma resistor. - Connect to VSS
VCOMR			This pin provides voltage reference for internal voltage regulator when register VDV[4:0] of Power Control 4 set to “01111”. - Connect to an external voltage source for reference
VCOMH	Output	Voltages for VCOM Signal	This pin indicates a HIGH level of VCOM generated in driving the VCOM alternation. - Connect a capacitor for stabilization
VCOML			This pin indicates a LOW level of VCOM generated in driving the VCOM alternation. - Connect a capacitor for stabilization

Name	I/O	Function	Description
VLCD63	Output	LCD Driving Voltages	Internal generated power for source driver - Connect a capacitor for stabilization
VGH			A positive power output pin for gate driver. - Connect a capacitor for stabilization
VGL			A negative power output pin for gate driver. - Connect a capacitor for stabilization
CP	Input	Booster and Stabilization Capacitors	- Connect a capacitor to CN
CXP			- Connect a capacitor to CXN
CYP			- Connect a capacitor to CYN
C1P			- Connect a capacitor to C1N
C2P			- Connect a capacitor to C2N
C3P			- Connect a capacitor to C3N
CN			- Connect a capacitor to CP
CXN			- Connect a capacitor to CXP
CYN			- Connect a capacitor to CYP
C1N			- Connect a capacitor to C1P
C2N			- Connect a capacitor to C2P
C3N			- Connect a capacitor to C3P
DRV	Output	PWM control	Power transistor gate signal for the boost converter
VFB	Input		Main boost regulator feedback input. Connect feedback resistive divider to GND. FB threshold is 0.6 V nominal
TEST4~5	Input	IC Testing Signal	Test pin of the internal circuit. Leave it connect to ground.
TEST6~17	Output	IC Testing Signal	Test pin of the internal circuit. Leave it OPEN.
VCOM	Output	LCD Driving Signals	A power supply for the TFT-display common electrode.
G0-G239			Gate driver output pins. These pins output VGH, VGL level.
S0-S959			Source driver output pins. S (3n) : display Red if BGR = LOW, Blue if BGR = HIGH. S (3n+1) : display Green. S (3n+2) : display Blue if BGR = LOW, Red if BGR = HIGH.
THROUGH1			Dummy pads. Used to measure the COG contact resistance. These two pins are short circuited within the chip
THROUGH2			
THROUGH3			Dummy pads. Used to measure the COG contact resistance. These two pins are short circuited within the chip
THROUGH4			
THROUGH5			Dummy pads. Used to measure the COG contact resistance. These two pins are short circuited within the chip
THROUGH6			
THROUGH7			Dummy pads. Used to measure the COG contact resistance. These two pins are short circuited within the chip
THROUGH8			
DUMMY			Floating pins and no connection inside the IC. These pins can be shorted together or connect to any signal.

7. Block Function Description

7.1 Serial Interface

The SPI is available through the chip select line (CSB), serial transfer clock line (SCK), serial data input (SDI), and serial data output (SDO).
The Driver IC recognizes the start of data transfer at the falling edge of CSB input to initiate the transfer of start byte. It recognizes the end of data transfer at the rising edge of CSB input. The Driver IC is selected when the 6-bit chip address in the start byte transferred from the transmission device and the 6-bit device identification code assigned to the Driver IC are compared and both 6-bit data correspond. The identification code must be 011100. Two different chip addresses must be assigned to the Driver IC because the seventh bit of the start byte is assigned to a register select bit (RS). When RS = 0, index register write or status read is executed. When the RS = 1, instruction write. The eighth bit of the start byte is to specify read or write (R/W bit). The data are received when the R/W bit is 0, and are transmitted when the R/W bit is 1.
After receiving the start byte, the Driver IC starts to transmit or receive data by byte. The data transmission adopts a format by which the MSB is first transmitted (9th SCK started). All Driver IC instructions consist of 16 bits and they are executed internally after two bytes are transmitted with the MSB first (IB15 to 0---9th ~24th SCK).

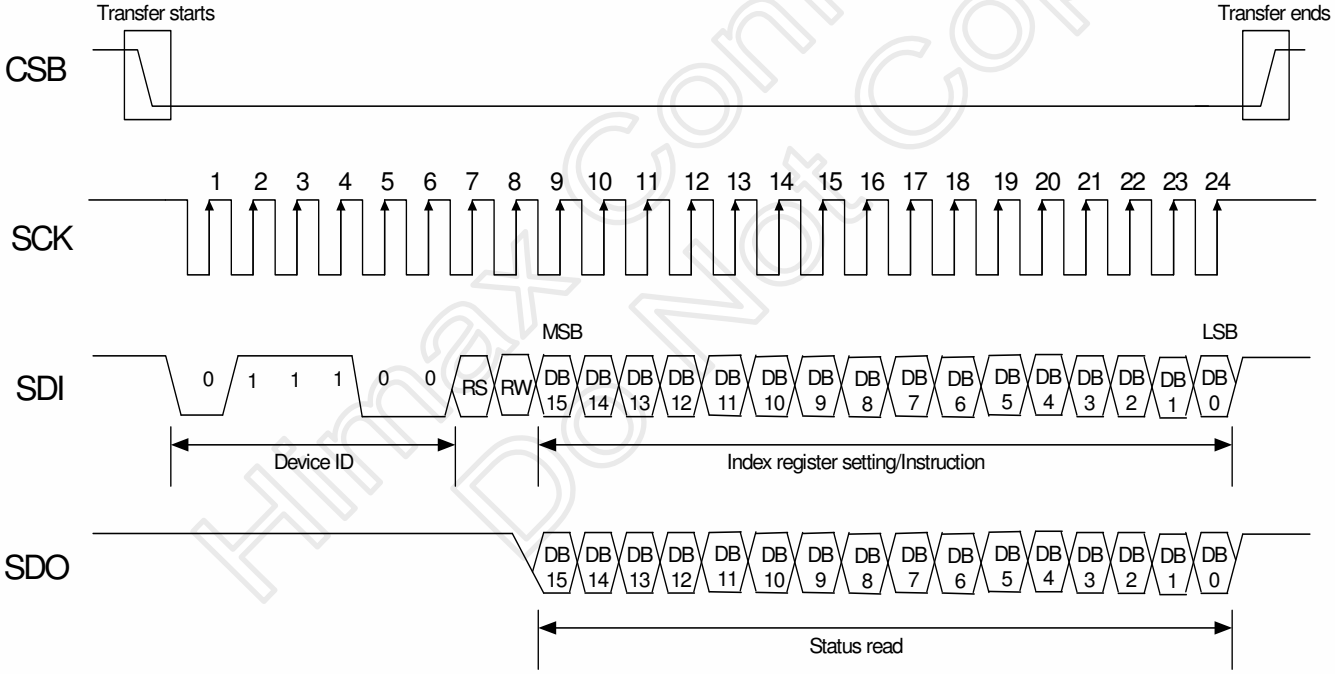


Figure 7. 1 SPI Timing

7.2 Data Control

The display data and frame position information from the controller is synchronized with the Gate Drive circuit and shift registered for the Source Driver circuit.

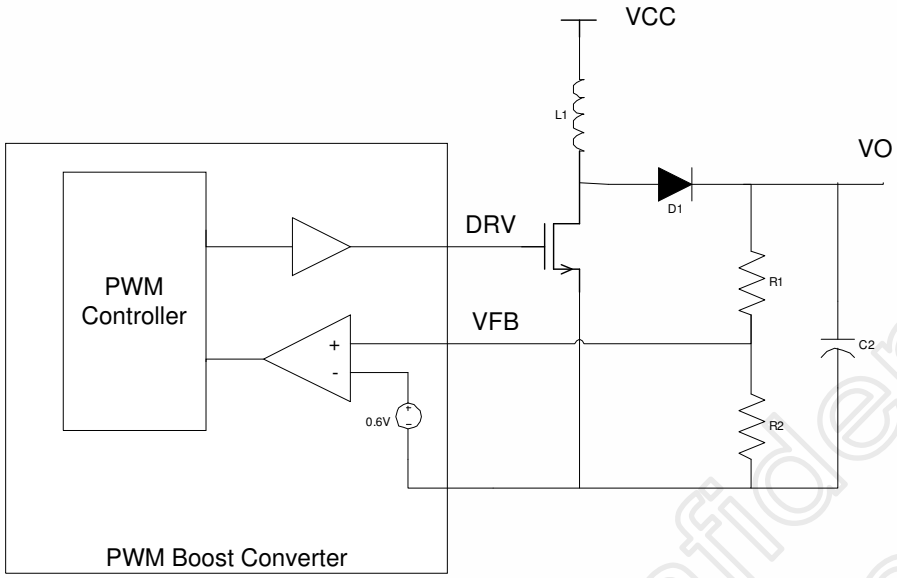
7.3 Gamma/Grayscale Voltage Generator

The grayscale voltage circuit generates a LCD driver circuit that corresponds to the grayscale levels as specified in the grayscale gamma-adjusting resistor. 262K possible colors can be displayed.

7.4 Boost and Regulator Circuit

These two functional blocks generate the voltage of VGH, VGL, VCOMH, VCOML and VLCD63, which are necessary for operating a TFT LCD.

7.5 PWM Boost Converter



The internal reference voltage is adjustable by FB[2:0] in R05h. By adjusting the voltage, you can get different VO to meet your system application.

7.6 Shift Register

The shift registers control the direction of line scanning of source.

7.7 Data Latches

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the Source Driver to output the required voltage level.

7.8 Aging Mode

If only DOTCLK is sent into driver IC without VSYNC, HSYNC, and DEN signals, HX8238-A will enter Aging Mode after power on. In Aging Mode, the display will show Black, White, Red, Green, and Blue images in series automatically.

7.9 Reset Circuit

This block is integrated into the Interface Logic which includes Power On Reset circuitry and the hardware reset pin, /RES. Both of these having the same reset function. Once the /RES pin receives a negative reset pulse, all internal circuitry will start to initialize. The minimum pulse width for completing the reset sequence is 10us. The status of the chip after reset is given by:

Reg#	Hex Code	Register Bit Value
R01h	XX00	RL = X REV = X PINV = X BGR = X SM = "0" TB = X CPE = X
R02h	0200	B/C = "1" NW = "00000000"
R03h	6364	DCT = "0110" BT = "011" BTF = "0" DC = "0110" AP = "010"
R04h	04XX	PALM = "1" BLT = "00" OEA = **note 2** SEL = X SWD = X
R05h		GHN="1" XDK="0" GDIS="1" LPF="1" DEP="0" CKP="1" VSP= **note 2** HSP="0" DEO="1" DIT="1" PWM="0" FB="100"
R0Ah	4008	BR = "1000000" CON = "01000"
R0Bh	D400	NO = "11" SDT = "01" EQ = "100"
R0Dh	3229	VRC = "011" VDS = "10" VRH = "101001"
R0Eh	3200	VCOMG = "1" VDV = "1001000"
R0Fh	0000	SCN = "00000000"
R16h	9F80	XLIM = "100111111"
R17h		STH = "00" HBP = **note 2** VBP = **note 2**
R1Eh	0052	nOTP = "0" VCM = "1010010"
R30h	0000	PKP1 = "000" PKP0 = "000"
R31h	0407	PKP3 = "100" PKP2 = "111"
R32h	0202	PKP5 = "010" PKP4 = "010"
R33h	0000	PRP1 = "000" PRP0 = "000"
R34h	0505	PKN1 = "101" PKN0 = "101"
R35h	0003	PKN3 = "000" PKN2 = "011"
R36h	0707	PKN5 = "111" PKN4 = "111"
R37h	0000	PRN1 = "000" PRN0 = "000"
R3Ah	0904	VRP1 = "01001" VRP0 = "0100"
R3Bh	0904	VRN1 = "01001" VRN0 = "0100"

Note 1 : X means the bit is refer to the logic stage of the corresponding hardware pin.
Note 2 : The default values of the VSP、OEA、HBP、VBP are automatically set by SEL.

Default Value auto setting			VSP	OEA[1:0]	HBP[6:0]	VBP[6:0]
SEL[2:0] = 000	NTSC		0	01	1000100	0010010
	PAL	PALM=0	0	01	1000100	0010010
		PALM=1				0010010
SEL[2:0] = 001	NTSC		0	01	1000100	0010010
	PAL	PALM=0	0	01	1000100	0010010
		PALM=1				0010010
SEL[2:0] = 010	NTSC		0	01	1000101	0010110
	PAL	PALM=0	0	10	1000101	0011100
		PALM=1				0011000
SEL[2:0] = 011	NTSC		0	01	1000100	0010110
	PAL	PALM=0	0	10	1000111	0011100
		PALM=1				0011000
SEL[2:0] = 100	NTSC		1	10	1000110	0010001
	PAL	PALM=0	1	10	1000110	0011000
		PALM=1				0010100
SEL[2:0] = 101	NTSC		1	10	1000101	0010001
	PAL	PALM=0	1	10	1001000	0011000
		PALM=1				0010100
SEL[2:0] = 110	NTSC		1	10	1000101	0010001
	PAL	PALM=0	1	10	1001000	0011000
		PALM=1				0010100
SEL[2:0] = 111	NTSC		1	10	1000110	0010001
	PAL	PALM=0	1	10	1000110	0011000
		PALM=1				0010100

Table 7. 1 Registers default value

8. Command Table

Reg#	Register	R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	PINV	BGR	SM	TB	CPE	0	0	0	0	0	0	0	0
R02h	LCD driver AC control	0	1	0	0	0	0	0	0	B/C	0	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
R04h	Data and color filter control	0	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	SWD2	SWD1	SWD0
R05h	Function control	0	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	PWM	0	FB2	FB1	FB0
R06h	Reserved	Reserved																	
R07h	Reserved	Reserved																	
R0Ah	Contrast/ Brightness control	0	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0
R0Dh	Power control (3)	0	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0
R0Fh	Gate scan starting Position	0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R16h	Horizontal Porch	0	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0
R17h	Vertical Porch	0	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R27h	Reserved	Reserved																	
R28h	Reserved	Reserved																	
R29h	Reserved	Reserved																	
R2Bh	Reserved	Reserved																	
R30h	γ control (1)	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R3Ah	γ control (9)	0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R3Bh	γ control (10)	0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

Note: * means don't care
Software settings will override hardware pin (eg, BGR bits override BGR pin definition)

Table 8. 1 Command table

9. Command Description

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	D5	ID4	ID3	ID2	ID1	ID0

Figure 9. 1 Index(IR)

The index instruction specifies the RAM control indexes (R00h to R7Fh). It sets the register number in the range of 0000000 to 1111111 in binary form. But do not access to Index register and instruction bits which do not have it's own index register.

Status Read

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Figure 9. 2 Status read

The status read instruction reads the internal status of the HX8238-A.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	R L	REV	PINV	BGR	S M	T B	CPE	0	0	1	1	1	1	1	1

Figure 9. 3 Driver output control

CPE: When CPE=0, internal charge pump circuit is shut down. When CPE=1, internal charge pump circuit is enabled.

REV: Displays all character and graphics display sections with reversal when REV = "1". Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below.

REV	RGB data	Source output level	
		VCOM = "H"	VCOM = "L"
0	00000H : 3FFFFH	V0 : V63	V63 : V0
1	00000H : 3FFFFH	V63 : V0	V0 : V63

Table 9. 1 Source output level

PINV: When PINV=0, POL output is same phase with internal VCOM signal. When PINV=1, POL output phase is reversed with VCOM signal.

BGR: Selects the <R><G><B> arrangement. When BGR = "0" <R><G><B> color is assigned from S0.When BGR = "1" <B><G><R> color is assigned from S0.

SM: Change the division of gate driver. When SM = "0", odd/even division (interlace mode) is selected. When SM = "1", upper/lower division is selected. Select the division mode according to the mounting method.

TB: Selects the output shift direction of the gate driver. When TB = "1", G0 shifts to G239. When TB = "0", G239 shifts to G0.

RL: Selects the output shift direction of the source driver. When RL = "1", S0 shifts to S959 and <R><G><B> color is assigned from S0. When RL = "0", S959 shifts to S0 and <R><G><B> color is assigned from S959. Set RL bit and BGR bit when changing the dot order of R, G and B.

Note: The default setting of register bits **REV**, **BGR**, **TB** and **RL** are defined by the logic stage of corresponding hardware pins. These bits will override the hardware setting once software command was sent to set the bits.

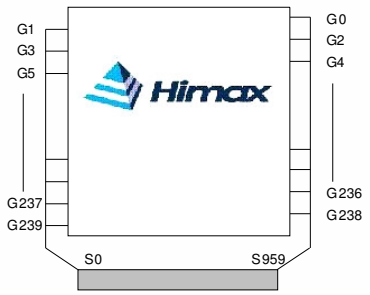
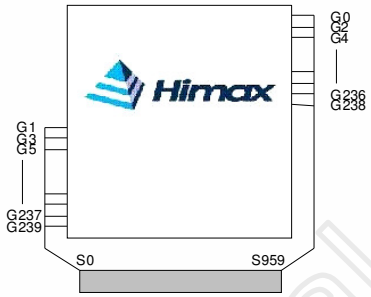
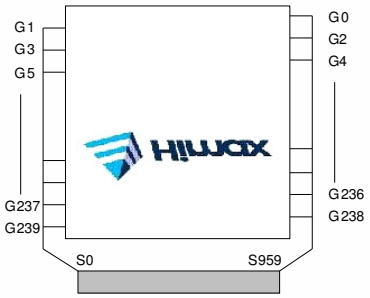
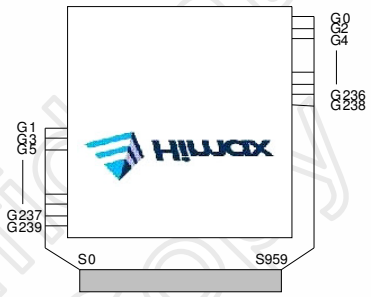
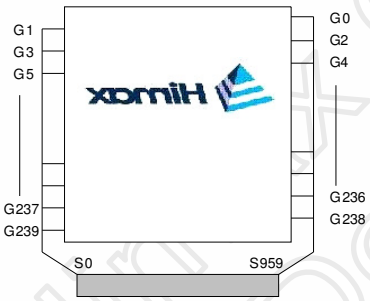
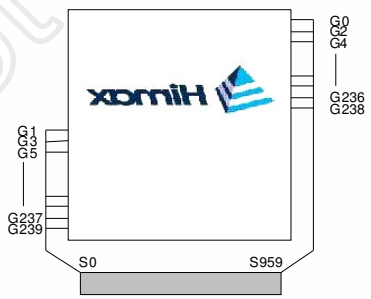
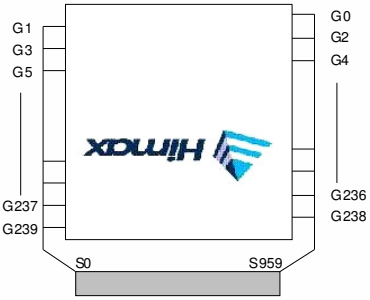
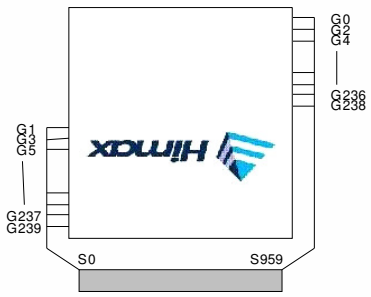
	SM = 0	SM = 1
TB = 1 **RL = 1**		
TB = 0 **RL = 1**		
TB = 1 **RL = 0**		
TB = 0 **RL = 0**		

Figure 9. 4 Scan direction & Display

LCD-Driving-Waveform Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	B/C	0	NW7	MW6	NW5	NW4	NW3	NW2	NW1	NW0

Figure 9. 5 LCD-driving-waveform control

B/C: When B/C = 0, frame inversion of the LCD driving signal is enabled. When B/C = 1, a N-line inversion waveform is generated and alternates in each N lines specified by bits NW7-0.

NW7-0: Specify the number of lines that will alternate at the N-line inversion setting (B/C = 1). NW7-0 alternate for every set value + 1 line.

Power control 1 (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DCT3	DCT2	DCT1	DCT0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0

Figure 9. 6 Power control 1

DCT3-0: Set the step-up cycle of the step-up circuit for 8-color mode (CM = VDDIO). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DCT3	DCT2	DCT1	DCT0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

* Fline = horizontal frequency (Fline Typ. 15KHz)

Table 9. 2 Step-up cycle

BT2-0 & BTF: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power supply voltage to be used.

BTF	BT2	BT1	BT0	VGH output	VGL output
0	0	0	0	V_{CIX2j} X 3	- (V_{CIX2j} X 3) + V_{CI}
0	0	0	1	V_{CIX2j} X 3	- (V_{CIX2j} X 2)
0	0	1	0	$V_{CIX2\ j}$ X 3	- (V_{CIX2j} X 3)
0	0	1	1	V_{CIX2j} X 2 + V_{CI}	- (V_{CIX2j} X 2) - V_{CI}
0	1	0	0	V_{CIX2j} X 2 + V_{CI}	- (V_{CIX2j} X 2)
0	1	0	1	V_{CIX2j} X 2 + V_{CI}	- (V_{CIX2j} X 2) + V_{CI}
0	1	1	0	V_{CIX2j} X 2	- (V_{CIX2j} X 2)
1	1	1	1	V_{CIX2j} X 2	- (V_{CIX2j} X 2) + V_{CI}
1	X	X	X	V_{CIX2j} X 3	- V_{CIX2j}

Table 9. 3 VGH and VGL booster ratio

DC3-0: Set the step-up cycle of the step-up circuit for 262k-color mode (CM = VSS). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

* Fline = horizontal frequency (Fline Typ. 15KHz)

Table 9. 4 Step-up cycle

AP2-0: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. During times when there is no display, such as when the system is in a sleep mode, set AP2-0 = “000” to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Large to Maximum
1	1	1	Maximum

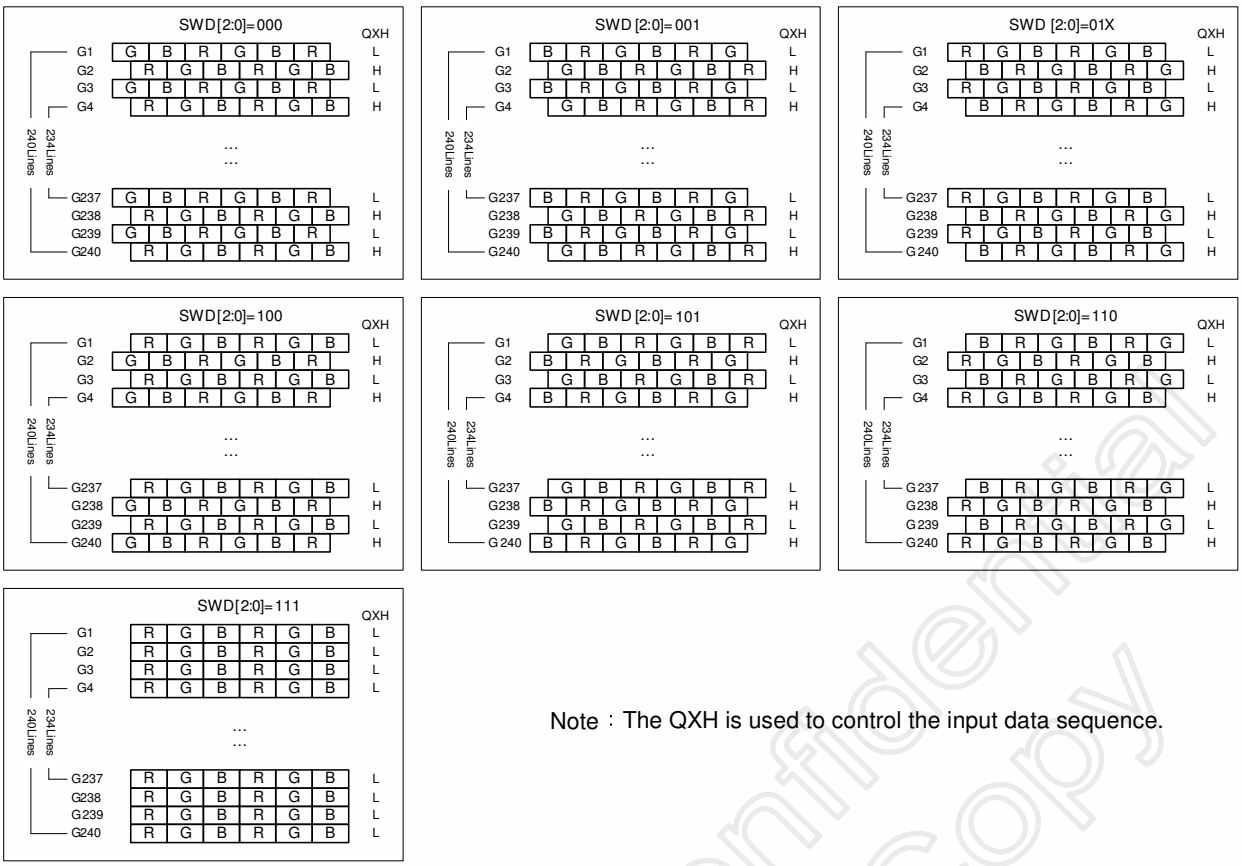
Table 9. 5 Op-amp power

Input Data and Color Filter Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	SWD2	SWD1	SWD0

Figure 9. 7 Input data and color filter control

SWD2-0: Control and switch the relationship between the R, G, B data and color filter type.



Note：The QXH is used to control the input data sequence.

Table 9. 6 Color filter type.

SEL2-0: Define the input interface mode.

SEL2	SEL1	SEL0	Format	Operating Frequency
0	0	0	Parallel-RGB data format (only support stripe type color filter)	6.5MHz
0	0	1	Serial-RGB data format	19.5MHz
0	1	0	CCIR 656 data format (640RGB)	24.54MHz
0	1	1	CCIR 656 data format (720RGB)	27MHz
1	0	0	YUV mode A data format (Cr-Y-Cb-Y)	24.54MHz
1	0	1	YUV mode A data format (Cr-Y-Cb-Y)	27MHz
1	1	0	YUV mode B data format (Cb-Y-Cr-Y)	27MHz
1	1	1	YUV mode B data format (Cb-Y-Cr-Y)	24.54MHz

Input format	DOTCLK Freq (MHz)	Display Data	Active Area (DOTCLK)
YUV mode	24.54	640	1280
	27	720	1440

Table 9. 7 Interface type.

OEA1-0: Odd/Even filed advanced function.

OEA1	OEA0	
0	0	Display Start @ VBP delay for Odd field and @ ***VBP-1*** for Even field.
0	1	Display Start @ VBP delay for Odd field and @ ***VBP*** for Even field.
1	0	Display Start @ VBP delay for Odd field and @ ***VBP+1*** for Even field.
1	1	No use

Table 9. 8 Odd/even filed advanced function.

BLT[1:0]: Set the initial power on black image insertion time.
00: 10 fields
01: 20 fields
10: 40 fields
11: 80 fields

PALM: Set the input data line number in PAL mode
0: 280 lines
1: 288 lines

Function Control (R05h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	PWM	0	FB2	FB1	FB0

Figure 9. 8 Function control

FB2-0: Set PWM feedback level adjustment.
000: 0.4V
001: 0.45V
010: 0.5V
011: 0.55V
100: 0.6V
101: 0.65V
110: 0.7V
111: 0.75V

PWM: When PWM=0, PWM function is disabled. When PWM=1, PWM function is enabled.

DIT: When DIT=0, dithering function is turned off. When DIT=1, dithering function is enabled.

DEO: When DEO=0, VSYNC/HSYNC are also needed in DE mode. Under this condition, vertical back porch is defined by VBP[6:0] and the horizontal first valid data is defined by DE signal. When DEO=1, only DEN signal is needed in DE mode.

HSP: When HSP=0, HSYNC is negative polarity. When HSP=1, HSYNC is positive polarity.

VSP: When VSP=0, VSYNC is negative polarity. When VSP=1, VSYNC is positive polarity.

CKP: When CKP=0, data is latched in CLK falling edge. When CKP=1, data is latched by CLK rising edge.

DEP: When DEP=0, DEN is negative polarity active. When DEP=1, DEN is positive polarity active.

LPF: When LPF=0, the low pass filter function in YUV mode is disabled. When LPF=1, the low pass filter function is YUV mode is enabled.

GDIS: When GDIS=0, VGL has no discharge path to VSS in standby mode. When GDIS=1, VGL will discharge to VSS in standby mode.

XDK: When XDK=0, VCIX2 is 2 stage pumping from VCI. (VCIX2=3 x VCI) When XDK=1, VCIX2 is 2 phase pumping from VCI. (VCIX2=2 x VCI)

GHN: When GHN=0, all gate outputs are forced to VGH. When GHN=1, gate driver is normal operation.

Contrast/Brightness Control (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0

Figure 9. 9 Contrast/Brightness control

CON4-0: Display Contrast level adjustment. (0.125/step) Adjust range from 00h(level = 0) to 1Fh(level = 3.875). Default value is 08h(level = 1).

BR6-0: Display Brightness level adjustment. (2/step) Adjust range from 00h(level = -128) to 7Fh(level = +126). Default value is 40h(level = 0).

Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0

Figure 9. 10 Frame cycle control

NO1-0: Sets amount of non-overlap of the gate output.

NO1	NO0	Amount of non-overlap
0	0	1.5 us
0	1	3 us
1	0	4.5 us
1	1	6 us

Table 9. 9 Amount of non-overlap

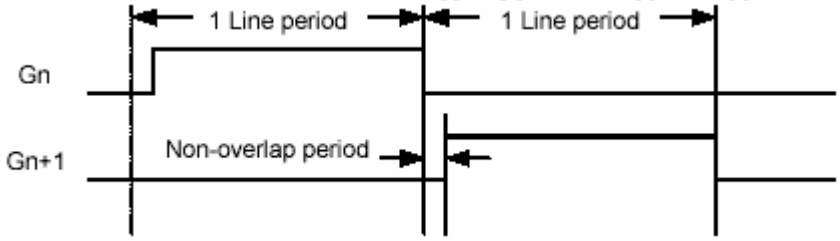


Figure 9. 11 **NO timing diagram**

SDT1-0: Set delay amount from the gate output signal falling edge to the source outputs.

SDT1	SDT0	Delay amount of the source output
0	0	1 us
0	1	3 us
1	0	5 us
1	1	7 us

Table 9. 10 Delay amount of the source output

EQ2-0: Sets the equalizing period.

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	3 us
0	1	0	4 us
0	1	1	5 us
1	0	0	6 us
1	0	1	7 us
1	1	0	8 us
1	1	1	9 us

Table 9. 11 EQ period

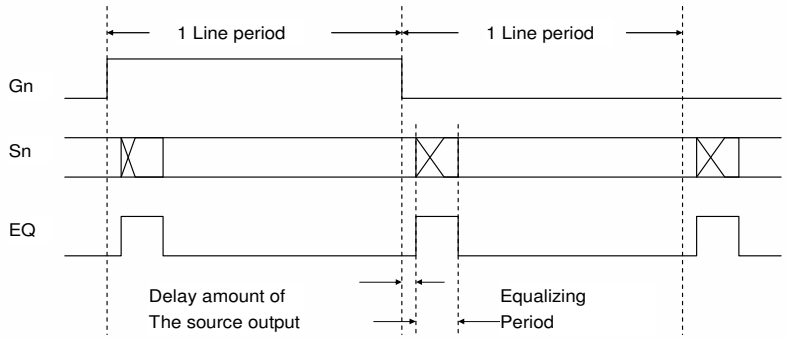


Figure 9. 12 EQ timing diagram

Power Control 2 (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0

Figure 9. 13 Power control 2

VRC[2:0]: set the VCIX2 charge pump voltage clamp.

VRC[2:0]=000, 5.1V
VRC[2:0]=001, 5.3V
VRC[2:0]=010, 5.5V
VRC[2:0]=011, 5.7V
VRC[2:0]=100, 5.9V
VRC[2:0]=101, reserved
VRC[2:0]=110, reserved
VRC[2:0]=111, reserved

VDS[1:0]: set the VDD regulator voltage if pin "REGVDD" is set to VDDIO.

VDS[1:0]=00, 1.8V
VDS[1:0]=01, 2V
VDS[1:0]=10, 2.2V
VDS[1:0]=11, 2.5V

VRH5-0: Set amplitude magnification of VLCD63. These bits amplify the VLCD63 voltage 2.464 to 4.456 times the Vref voltage set by VRH5-0.

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VLCD63Voltage		VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VLCD63Voltage
0	0	0	0	0	0	Vref x 2.456		1	0	0	0	0	0	Vref x 3.480
0	0	0	0	0	1	Vref x 2.488		1	0	0	0	0	1	Vref x 3.512
0	0	0	0	1	0	Vref x 2.520		1	0	0	0	1	0	Vref x 3.544
0	0	0	0	1	1	Vref x 2.552		1	0	0	0	1	1	Vref x 3.576
0	0	0	1	0	0	Vref x 2.584		1	0	0	1	0	0	Vref x 3.608
0	0	0	1	0	1	Vref x 2.616		1	0	0	1	0	1	Vref x 3.640
0	0	0	1	1	0	Vref x 2.648		1	0	0	1	1	0	Vref x 3.672
0	0	0	1	1	1	Vref x 2.680		1	0	0	1	1	1	Vref x 3.704
0	0	1	0	0	0	Vref x 2.712		1	0	1	0	0	0	Vref x 3.736
0	0	1	0	0	1	Vref x 2.744		1	0	1	0	0	1	Vref x 3.768
0	0	1	0	1	0	Vref x 2.776		1	0	1	0	1	0	Vref x 3.800
0	0	1	0	1	1	Vref x 2.808		1	0	1	0	1	1	Vref x 3.832
0	0	1	1	0	0	Vref x 2.840		1	0	1	1	0	0	Vref x 3.864
0	0	1	1	0	1	Vref x 2.872		1	0	1	1	0	1	Vref x 3.896
0	0	1	1	1	0	Vref x 2.904		1	0	1	1	1	0	Vref x 3.928
0	0	1	1	1	1	Vref x 2.936		1	0	1	1	1	1	Vref x 3.960

0	1	0	0	0	0	Vref x 2.968	1	1	0	0	0	0	Vref x 3.992
0	1	0	0	0	1	Vref x 3.000	1	1	0	0	0	1	Vref x 4.024
0	1	0	0	1	0	Vref x 3.032	1	1	0	0	1	0	Vref x 4.056
0	1	0	0	1	1	Vref x 3.064	1	1	0	0	1	1	Vref x 4.088
0	1	0	1	0	0	Vref x 3.096	1	1	0	1	0	0	Vref x 4.120
0	1	0	1	0	1	Vref x 3.128	1	1	0	1	0	1	Vref x 4.152
0	1	0	1	1	0	Vref x 3.160	1	1	0	1	1	0	Vref x 4.184
0	1	0	1	1	1	Vref x 3.192	1	1	0	1	1	1	Vref x 4.216
0	1	1	0	0	0	Vref x 3.224	1	1	1	0	0	0	Vref x 4.248
0	1	1	0	0	1	Vref x 3.256	1	1	1	0	0	1	Vref x 4.280
0	1	1	0	1	0	Vref x 3.288	1	1	1	0	1	0	Vref x 4.312
0	1	1	0	1	1	Vref x 3.320	1	1	1	0	1	1	Vref x 4.344
0	1	1	1	0	0	Vref x 3.352	1	1	1	1	0	0	Vref x 4.376
0	1	1	1	0	1	Vref x 3.384	1	1	1	1	0	1	Vref x 4.408
0	1	1	1	1	0	Vref x 3.416	1	1	1	1	1	0	Vref x 4.440
0	1	1	1	1	1	Vref x 3.448	1	1	1	1	1	1	Vref x 4.472

*Vref is the internal reference voltage equals to 1.25V.

Table 9. 12 VLCD63 voltage

Power Control 3 (R0Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VCOMG	VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0

Figure 9. 14 Power control 3

VCOMG: When VCOMG = “1”, it is possible to set output voltage of VCOML to any level, and the instruction (VDV6-0) becomes available. When VCOMG = “0”, VCOML output is fixed to VSS level, VCIM output for VCOML power supply stops, and the instruction (VDV6-0) becomes unavailable. Set VCOMG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

VDV6-0: Set the alternating amplitudes of VCOM at the VCOM alternating drive. These bits amplify VCOM amplitude 0.6 to 1.2525 times the VLCD63 voltage. When VCOMG = “0”, the settings become invalid. External voltage at VCOMR is referenced when VDV = “01111xx”.

VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude
0	0	0	0	0	0	0	VLCD63 x 0.6000
0	0	0	0	0	0	1	VLCD63 x 0.6075
0	0	0	0	0	1	0	VLCD63 x 0.6150
0	0	0	0	0	1	1	VLCD63 x 0.6225
0	0	0	0	1	0	0	VLCD63 x 0.6300
			:				: Step = 0.0075 :
0	1	1	1	0	1	0	VLCD63 x 1.0350
0	1	1	1	0	1	1	VLCD63 x 1.0425
0	1	1	1	1	*	*	Reference from external voltage (VCOMR)
1	0	0	0	0	0	0	VLCD63 x 1.0500
1	0	0	0	0	0	1	VLCD63 x 1.0575
			:				: Step = 0.0075 :
1	0	1	1	0	1	0	VLCD63 x 1.2450
1	0	1	1	0	1	1	VLCD63 x 1.2525
1	0	1	1	1	*	*	Reserved
1	1	*	*	*	*	*	Reserved

Table 9. 13 VCOM amplitude

Gate Scan Position (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

Figure 9. 15 Gate scan position

SCN8-0: Set the scanning starting position of the gate driver.

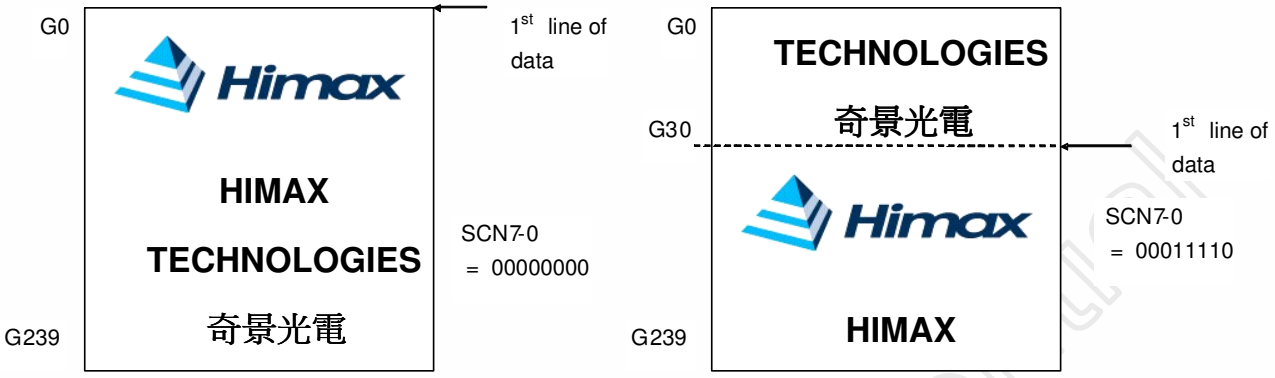


Figure 9. 16 Gate scan display position

Horizontal Porch (R16h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0

Figure 9. 17 Horizontal Porch

XLIM8-0: Set the number of valid pixel per line.

XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	No. of pixel per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
				:					: Step = 1 :
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320
1	0	1	*	*	*	*	*	*	Reserved
1	1	*	*	*	*	*	*	*	Reserved

Table 9. 14 No. of pixel per line

Vertical Porch (R17h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

Figure 9. 18 Vertical porch

HBP6-0: Set the delay period from falling edge of HSYNC signal to first valid data. The pixel data exceed the range set by XLIM8-0 and before the first valid data will be treated as dummy data. The setting is only effective in SYNC mode timing.

HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle
0	0	0	0	0	0	0	Can't set
0	0	0	0	0	0	1	Can't set
0	0	0	0	0	1	0	Can't set
0	0	0	0	0	1	1	Can't set
0	0	0	0	1	0	0	Can't set
0	0	0	0	1	0	1	Can't set
0	0	0	0	1	1	0	Can't set
0	0	0	0	1	1	1	Can't set
0	0	0	1	0	0	0	Can't set
0	0	0	1	0	0	1	9
							: Step = 1 :
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Table 9. 15 No. of clock cycle of clock

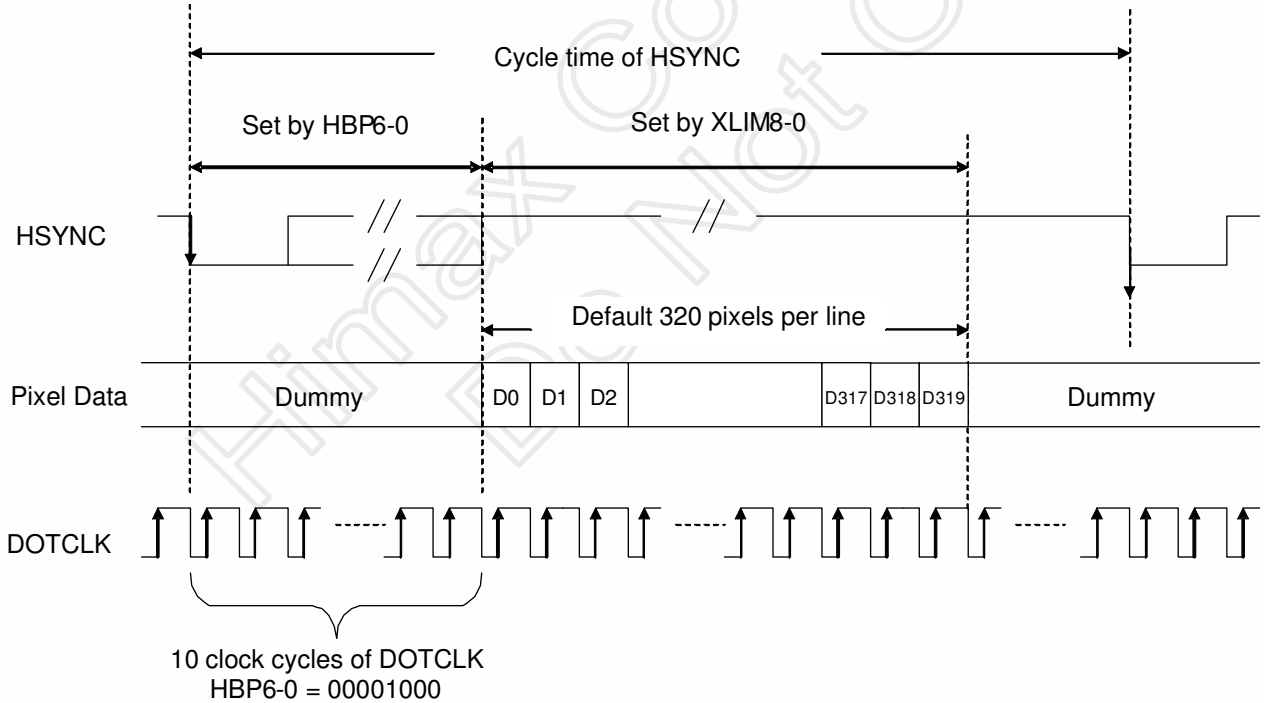


Figure 9. 19 **No. of clock cycle of clock**

STH1-0: Adjust the first valid data by dot clock. This setting is not valid in parallel RGB input interface.

STH = 00: +0 dot clock
STH = 01: +1 dot clock
STH = 10: +2 dot clock
STH = 11: +3 dot clock

VBP6-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line. The setting is only effective in SYNC mode timing.

VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	Can't set
0	0	0	0	0	0	1	Can't set
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
							: Step = 1 :
1	1	1	1	1	0	0	124
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Table 9. 16 No. of clock cycle of HSYNC

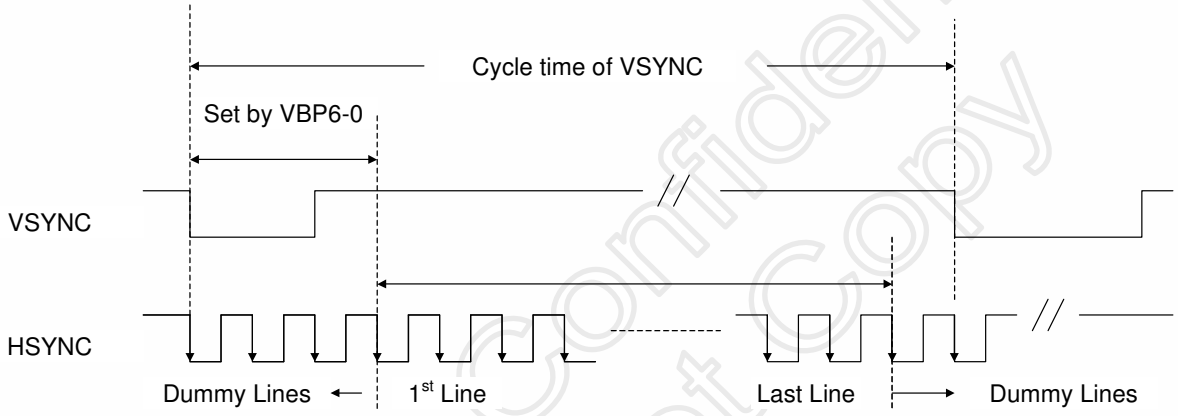


Figure 9. 20 No. of clock cycle of HSYNC

Power Control 4 (R1Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 9. 21 Power control 4

nOTP: nOTP equals to "0" after power on reset and VCOMH voltage equals to programmed OTP value. When nOTP set to "1", setting of VCM6-0 becomes valid and voltage of VCOMH can be adjusted.

VCM6-0: Set the VCOMH voltage if nOTP = "1". These bits amplify the VCOMH voltage 0.36 to 0.995 times the VLCD63 voltage.

VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	0	VLCD63 x 0.360
0	0	0	0	0	0	1	VLCD63 x 0.365
0	0	0	0	0	1	0	VLCD63 x 0.370
0	0	0	0	0	1	1	VLCD63 x 0.375
0	0	0	0	1	0	0	VLCD63 x 0.380
			:			:	: Step = 0.005 :
1	1	1	1	1	0	0	VLCD63 x 0.980
1	1	1	1	1	0	1	VLCD63 x 0.985
1	1	1	1	1	1	0	VLCD63 x 0.990
1	1	1	1	1	1	1	VLCD63 x 0.995

Note: $2V < V_{COMH} < V_{LCD63}$

Table 9. 17 VCOMH

Gamma Control 1 (R30h to R37h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1	PKP1	PKP1	0	0	0	0	0	PKP0	PKP0	PKP0
W	1	0	0	0	0	0	PKP3	PKP3	PKP3	0	0	0	0	0	PKP2	PKP2	PKP2
W	1	0	0	0	0	0	PKP5	PKP5	PKP5	0	0	0	0	0	PKP4	PKP4	PKP4
W	1	0	0	0	0	0	PRP1	PRP1	PRP1	0	0	0	0	0	PRP0	PRP0	PRP0
W	1	0	0	0	0	0	PKN1	PKN1	PKN1	0	0	0	0	0	PKN0	PKN0	PKN0
W	1	0	0	0	0	0	PKN3	PKN3	PKN3	0	0	0	0	0	PKN2	PKN2	PKN2
W	1	0	0	0	0	0	PKN5	PKN5	PKN5	0	0	0	0	0	PKN4	PKN4	PKN4
W	1	0	0	0	0	0	PRN1	PRN1	PRN1	0	0	0	0	0	PRN0	PRN0	PRN0

Figure 9. 22 Gamma control 1

PKP52–00: Gamma micro adjustment register for the positive polarity output.
PRP12-00: Gradient adjustment register for the positive polarity output.
PKN52-00: Gamma micro adjustment register for the negative polarity output.
PRN12-00: Gradient adjustment register for the negative polarity output.

Gamma Control 2 (R3Ah to R3Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
W	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00

Figure 9. 23 Gamma control 2

VRP14-00: Adjustment register for amplification adjustment of the positive polarity output.
VRN14-00: Adjustment register for the amplification adjustment of the negative polarity output.
(Refer to Gamma Adjustment Function for details)

10. OTP Programming

OTP write sequence

Step	Operation
1	Power up the module. Set nOTP=1 and find out the appropriate value of VCM[6:0] and power off the system
2	Power up the system with VDD=VDDIO=2.5V. If REGVDD=1, set R0Dh=16'h0324.
3	Set appropriate values found from step 1 to register of VCOM (R1Eh)
4	Set R06h=16'h2820 to stop VGH/VGL pumping. Wait 0.5s.
5	Set R60h=16'h8000
6	Set R60h=16'hC000
7	Connect 7.5V to VGH and 0V to VGL
8	Set R60h=16'hC200
9	Set R60h=16'hC280
10	Wait 200us for completing this program
11	Set R60h=16'hC200
12	Remove 7.5V from VGH and 0V from VGL
13	Set R60h=16'h8200
14	Set R60h=16'h0200
15	Set R60h=16'h0040
16	Set R60h=16'h0000

Table 10. 1 OTP Programming sequence

You can use above programming sequence to set VCM[6:0] value to OTP cell twice. If you want to check if the OTP cell is till available for programming, you can read the status from R61h shown below.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	0	0	0	0	0	0	0	0	IND	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 10. 1 OTP read table

You can check the IND bit to see if the VCM[6:0] is still programmable or not. If IND=0, you can program new VCM[6:0] value to OTP. If IND=1, it means that the OTP cell have already programmed twice and you can't program it any more. IB6~IB0 indicate the currently effective VCM[6:0] setting in OTP cell.

OTP Programming circuitry

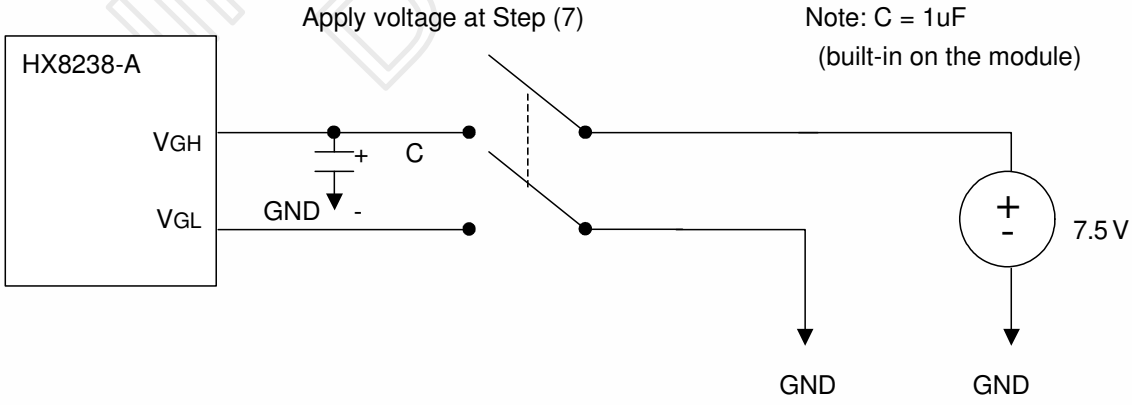


Figure 10. 2 OTP programming circuitry

11. Gamma Adjustment Function

The HX8238-A incorporates gamma adjustment function for the 262K-color display. Gamma adjustment is implemented by deciding the 8-grayscale levels with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.

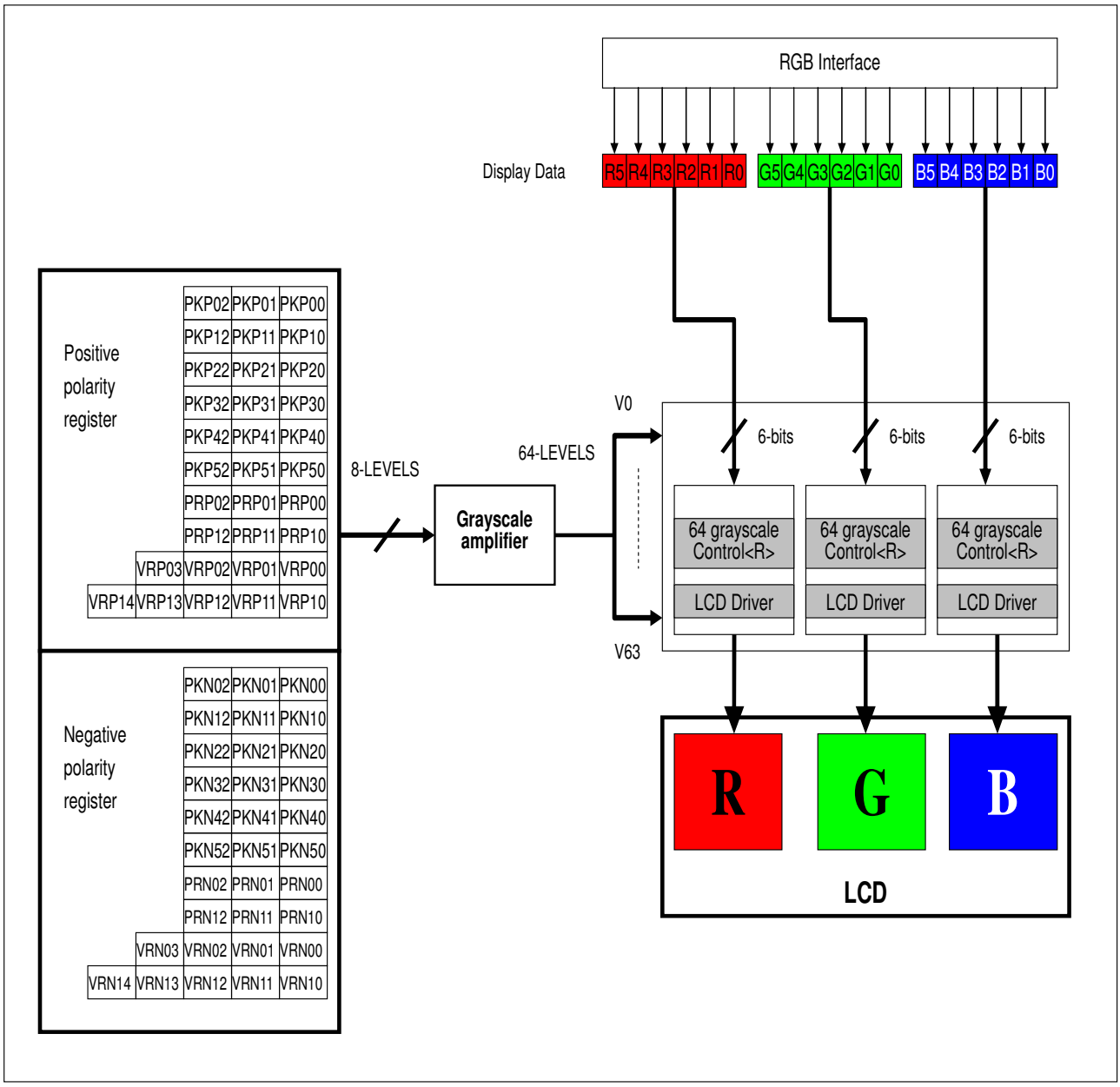


Figure 11. 1 Grayscale control block

11.1 Structure of Grayscale Amplifier

Below figure indicates the structure of the grayscale amplifier. It determines 8 levels (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V63.

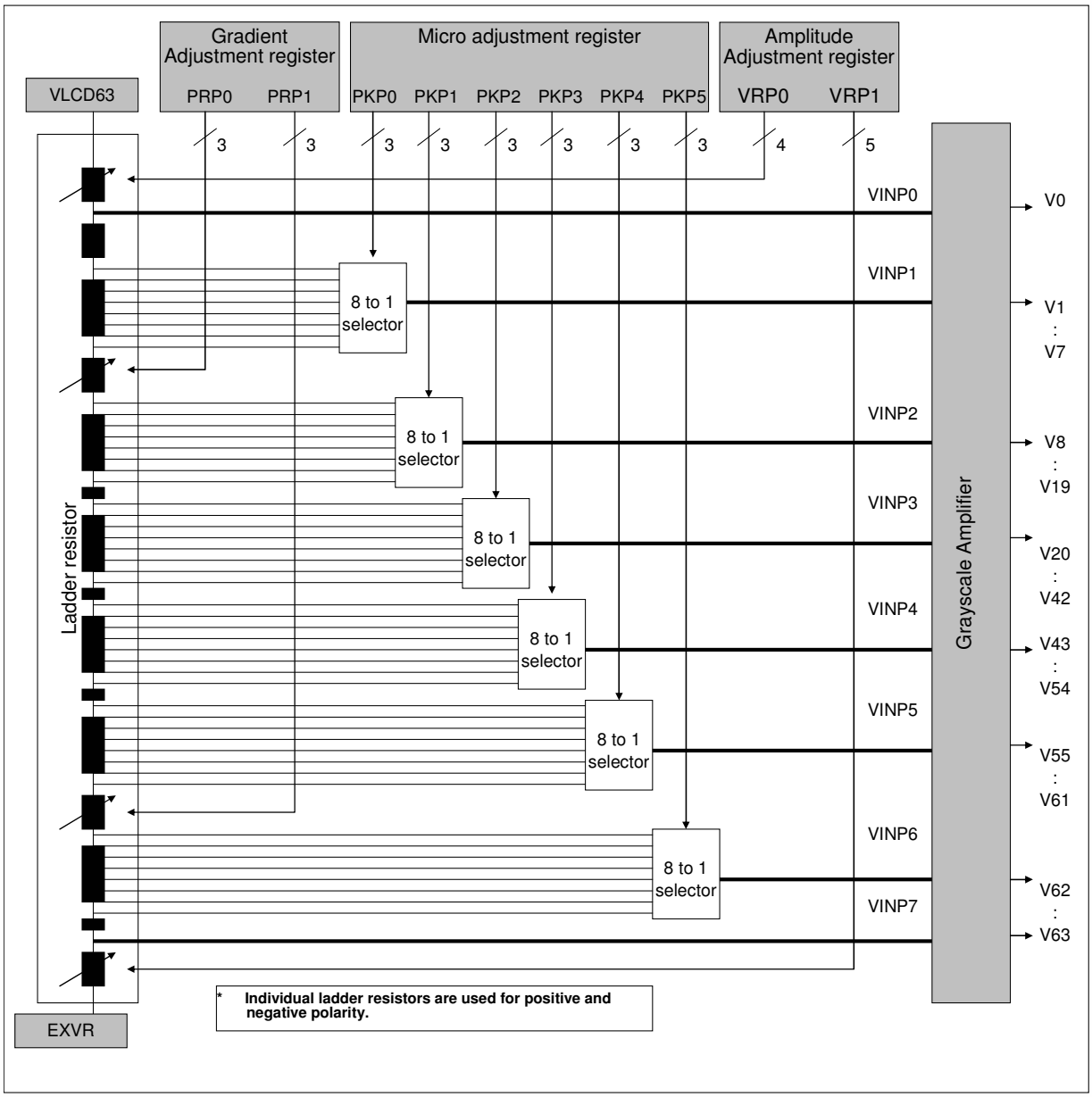


Figure 11. 2 Grayscale amplifier

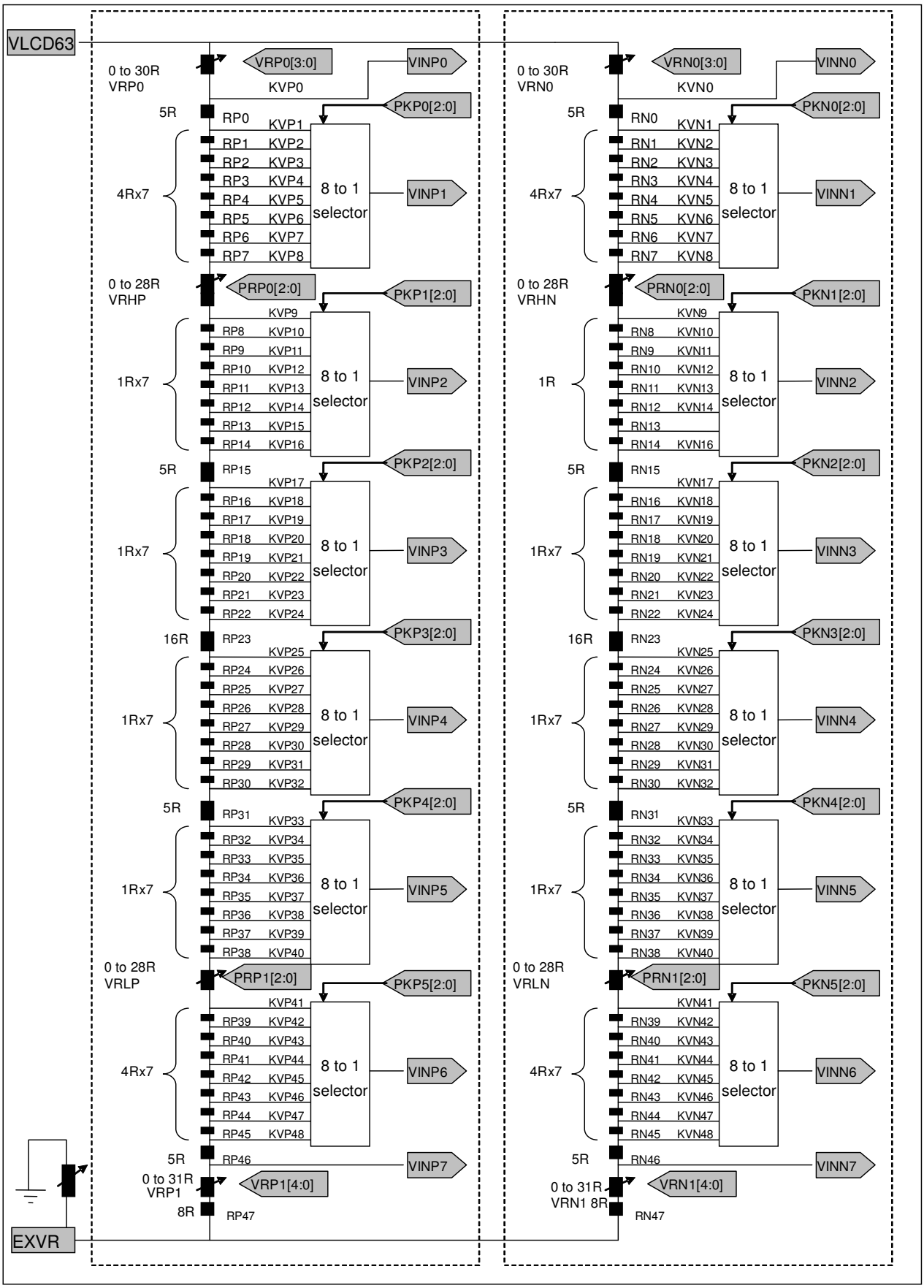


Figure 11. 3 Resistor ladder for gamma voltages generation

11.2 Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Using the same setting for Reference-value and R.G.B.) Following graphics indicates the operation of each adjusting register.

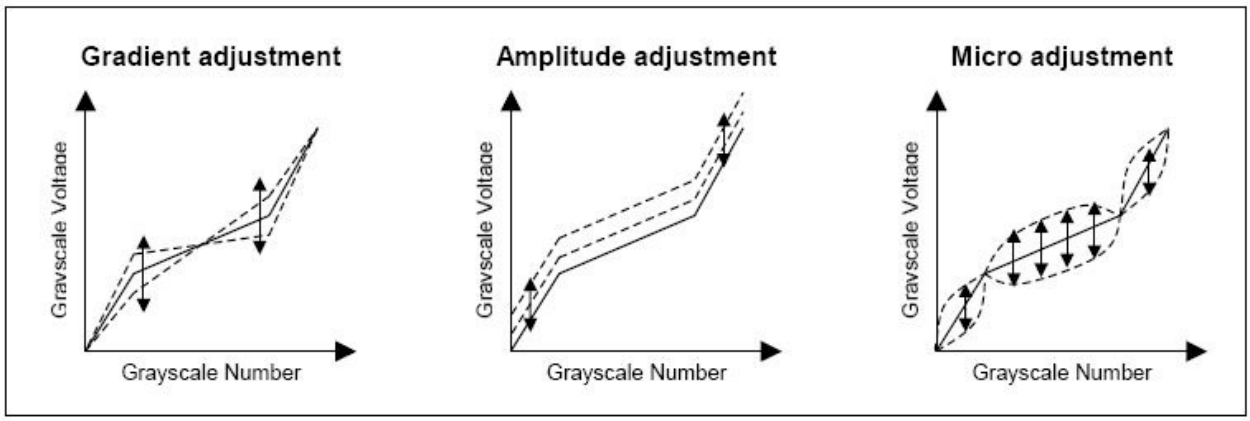


Figure 11. 4 Gamma adjustment function

11.2.1 Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP(N)0 / PRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

11.2.2 Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP(N)0 / VRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

11.2.3 Micro adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

11.3 Ladder Resistor / 8 to 1 selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors. Also, there has pin (EXVR) that can be connected to VSS or an external variable resistor for compensating the dispersion of length between one panel to another.

Variable Resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP(N)0 / PRP(N)1) and (VRP(N)0 / VRP(N)1) as below.

PRP(N)[0:1]	Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 11. 1 PRP(N)

VRP(N)0	Resistance
0000	0R
0001	2R
0010	4R
: Step = 2R :	
1110	28R
1111	30R

Table 11. 2 VRP(N)0

VRP(N)1	Resistance
00000	0R
00001	1R
00010	2R
: Step = 1R :	
11110	30R
11111	31R

Table 11. 3 VRP(N)1

8 to 1 selector

In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are six types of reference voltage (VIN1 to VIN6) and totally 48 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro adjusting register and the selecting voltage.

Positive polarity							Negative polarity						
Register PKP[2:0]	Selected voltage						Register PKN[2:0]	Selected voltage					
	VINP1	VINP2	VINP3	VINP4	VINP5	VINP6		VINN1	VINN2	VINN3	VINN4	VINN5	VINN6
000	KVP1	KVP9	KVP17	KVP25	KVP33	KVP41	000	KVN1	KVN9	KVN17	KVN25	KVN33	KVN41
001	KVP2	KVP10	KVP18	KVP26	KVP34	KVP42	001	KVN2	KVN10	KVN18	KVN26	KVN34	KVN42
010	KVP3	KVP11	KVP19	KVP27	KVP35	KVP43	010	KVN3	KVN11	KVN19	KVN27	KVN35	KVN43
011	KVP4	KVP12	KVP20	KVP28	KVP36	KVP44	011	KVN4	KVN12	KVN20	KVN28	KVN36	KVN44
100	KVP5	KVP13	KVP21	KVP29	KVP37	KVP45	100	KVN5	KVN13	KVN21	KVN29	KVN37	KVN45
101	KVP6	KVP14	KVP22	KVP30	KVP38	KVP46	101	KVN6	KVN14	KVN22	KVN30	KVN38	KVN46
110	KVP7	KVP15	KVP23	KVP31	KVP39	KVP47	110	KVN7	KVN15	KVN23	KVN31	KVN39	KVN47
111	KVP8	KVP16	KVP24	KVP32	KVP40	KVP48	111	KVN8	KVN16	KVN24	KVN32	KVN40	KVN48

Table 11. 4 PKP and PKN

Grayscale voltage	Positive Polarity	Negative Polarity
V0	VINP0	VINN7
V1	VINP1	VINN6
V2	V8+(V1-V8)*(2241/2703)	V1+(V8-V1)*(462/2703)
V3	V8+(V1-V8)*(1671/2703)	V1+(V8-V1)*(1032/2703)
V4	V8+(V1-V8)*(1209/2703)	V1+(V8-V1)*(1494/2703)
V5	V8+(V1-V8)*(849/2703)	V1+(V8-V1)*(1854/2703)
V6	V8+(V1-V8)*(567/2703)	V1+(V8-V1)*(2136/2703)
V7	V8+(V1-V8)*(294/2703)	V1+(V8-V1)*(2409/2703)
V8	VINP2	VINN5
V9	V20+(V8-V20)*(1533/1767)	V8+(V20-V8)*(234/1767)
V10	V20+(V8-V20)*(1356/1767)	V8+(V20-V8)*(411/1767)
V11	V20+(V8-V20)*(1188/1767)	V8+(V20-V8)*(579/1767)
V12	V20+(V8-V20)*(993/1767)	V8+(V20-V8)*(774/1767)
V13	V20+(V8-V20)*(843/1767)	V8+(V20-V8)*(924/1767)
V14	V20+(V8-V20)*(693/1767)	V8+(V20-V8)*(1074/1767)
V15	V20+(V8-V20)*(543/1767)	V8+(V20-V8)*(1224/1767)
V16	V20+(V8-V20)*(441/1767)	V8+(V20-V8)*(1326/1767)
V17	V20+(V8-V20)*(336/1767)	V8+(V20-V8)*(1431/1767)
V18	V20+(V8-V20)*(213/1767)	V8+(V20-V8)*(1554/1767)
V19	V20+(V8-V20)*(81/1767)	V8+(V20-V8)*(1686/1767)
V20	VINP3	VINN4
V21	V43+(V20-V43)*(1887/1965)	V20+(V43-V20)*(78/1965)
V22	V43+(V20-V43)*(1779/1965)	V20+(V43-V20)*(186/1965)
V23	V43+(V20-V43)*(1653/1965)	V20+(V43-V20)*(312/1965)
V24	V43+(V20-V43)*(1536/1965)	V20+(V43-V20)*(429/1965)
V25	V43+(V20-V43)*(1437/1965)	V20+(V43-V20)*(528/1965)
V26	V43+(V20-V43)*(1362/1965)	V20+(V43-V20)*(603/1965)
V27	V43+(V20-V43)*(1278/1965)	V20+(V43-V20)*(687/1965)
V28	V43+(V20-V43)*(1191/1965)	V20+(V43-V20)*(774/1965)
V29	V43+(V20-V43)*(1098/1965)	V20+(V43-V20)*(867/1965)
V30	V43+(V20-V43)*(1008/1965)	V20+(V43-V20)*(957/1965)
V31	V43+(V20-V43)*(927/1965)	V20+(V43-V20)*(1038/1965)
V32	V43+(V20-V43)*(843/1965)	V20+(V43-V20)*(1122/1965)
V33	V43+(V20-V43)*(750/1965)	V20+(V43-V20)*(1215/1965)
V34	V43+(V20-V43)*(678/1965)	V20+(V43-V20)*(1287/1965)
V35	V43+(V20-V43)*(612/1965)	V20+(V43-V20)*(1353/1965)
V36	V43+(V20-V43)*(528/1965)	V20+(V43-V20)*(1437/1965)
V37	V43+(V20-V43)*(450/1965)	V20+(V43-V20)*(1515/1965)
V38	V43+(V20-V43)*(375/1965)	V20+(V43-V20)*(1590/1965)
V39	V43+(V20-V43)*(303/1965)	V20+(V43-V20)*(1662/1965)
V40	V43+(V20-V43)*(222/1965)	V20+(V43-V20)*(1743/1965)
V41	V43+(V20-V43)*(147/1965)	V20+(V43-V20)*(1818/1965)
V42	V43+(V20-V43)*(87/1965)	V20+(V43-V20)*(1878/1965)
V43	VINP4	VINN3
V44	V55+(V43-V55)*(936/1014)	V43+(V55-V43)*(78/1014)
V45	V55+(V43-V55)*(867/1014)	V43+(V55-V43)*(147/1014)
V46	V55+(V43-V55)*(792/1014)	V43+(V55-V43)*(222/1014)
V47	V55+(V43-V55)*(723/1014)	V43+(V55-V43)*(291/1014)
V48	V55+(V43-V55)*(648/1014)	V43+(V55-V43)*(366/1014)
V49	V55+(V43-V55)*(561/1014)	V43+(V55-V43)*(453/1014)
V50	V55+(V43-V55)*(465/1014)	V43+(V55-V43)*(549/1014)
V51	V55+(V43-V55)*(387/1014)	V43+(V55-V43)*(627/1014)
V52	V55+(V43-V55)*(291/1014)	V43+(V55-V43)*(723/1014)
V53	V55+(V43-V55)*(201/1014)	V43+(V55-V43)*(813/1014)
V54	V55+(V43-V55)*(111/1014)	V43+(V55-V43)*(903/1014)
V55	VINP5	VINN2
V56	V62+(V55-V62)*(1218/1317)	V55+(V62-V55)*(99/1317)
V57	V62+(V55-V62)*(1092/1317)	V55+(V62-V55)*(225/1317)
V58	V62+(V55-V62)*(936/1317)	V55+(V62-V55)*(381/1317)
V59	V62+(V55-V62)*(774/1317)	V55+(V62-V55)*(543/1317)
V60	V62+(V55-V62)*(579/1317)	V55+(V62-V55)*(738/1317)
V61	V62+(V55-V62)*(324/1317)	V55+(V62-V55)*(993/1317)
V62	VINP6	VINN1
V63	VINP7	VINN0

Table 11. 5 Grayscale voltages formulas

Reference	Formula	Micro-adjusting register	Reference voltage
KVP0	VLCD63 - ΔV x VRP0 / SUMRP	-	VINP0
KVP1	VLCD63 - ΔV x (VRP0 + 5R) / SUMRP	PKP0[2:0] = ”000”	VINP1
KVP2	VLCD63 - ΔV x (VRP0 + 9R) / SUMRP	PKP0[2:0] = ”001”	
KVP3	VLCD63 - ΔV x (VRP0 + 13R) / SUMRP	PKP0[2:0] = ”010”	
KVP4	VLCD63 - ΔV x (VRP0 + 17R) / SUMRP	PKP0[2:0] = ”011”	
KVP5	VLCD63 - ΔV x (VRP0 + 21R) / SUMRP	PKP0[2:0] = ”100”	
KVP6	VLCD63 - ΔV x (VRP0 + 25R) / SUMRP	PKP0[2:0] = ”101”	
KVP7	VLCD63 - ΔV x (VRP0 + 29R) / SUMRP	PKP0[2:0] = ”110”	
KVP8	VLCD63 - ΔV x (VRP0 + 33R) / SUMRP	PKP0[2:0] = ”111”	
KVP9	VLCD63 - ΔV x (VRP0 + 33R + VRHP) / SUMRP	PKP1[2:0] = ”000”	VINP2
KVP10	VLCD63 - ΔV x (VRP0 + 34R + VRHP) / SUMRP	PKP1[2:0] = ”001”	
KVP11	VLCD63 - ΔV x (VRP0 + 35R + VRHP) / SUMRP	PKP1[2:0] = ”010”	
KVP12	VLCD63 - ΔV x (VRP0 + 36R + VRHP) / SUMRP	PKP1[2:0] = ”011”	
KVP13	VLCD63 - ΔV x (VRP0 + 37R + VRHP) / SUMRP	PKP1[2:0] = ”100”	
KVP14	VLCD63 - ΔV x (VRP0 + 38R + VRHP) / SUMRP	PKP1[2:0] = ”101”	
KVP15	VLCD63 - ΔV x (VRP0 + 39R + VRHP) / SUMRP	PKP1[2:0] = ”110”	
KVP16	VLCD63 - ΔV x (VRP0 + 40R + VRHP) / SUMRP	PKP1[2:0] = ”111”	
KVP17	VLCD63 - ΔV x (VRP0 + 45R + VRHP) / SUMRP	PKP2[2:0] = ”000”	VINP3
KVP18	VLCD63 - ΔV x (VRP0 + 46R + VRHP) / SUMRP	PKP2[2:0] = ”001”	
KVP19	VLCD63 - ΔV x (VRP0 + 47R + VRHP) / SUMRP	PKP2[2:0] = ”010”	
KVP20	VLCD63 - ΔV x (VRP0 + 48R + VRHP) / SUMRP	PKP2[2:0] = ”011”	
KVP21	VLCD63 - ΔV x (VRP0 + 49R + VRHP) / SUMRP	PKP2[2:0] = ”100”	
KVP22	VLCD63 - ΔV x (VRP0 + 50R + VRHP) / SUMRP	PKP2[2:0] = ”101”	
KVP23	VLCD63 - ΔV x (VRP0 + 51R + VRHP) / SUMRP	PKP2[2:0] = ”110”	
KVP24	VLCD63 - ΔV x (VRP0 + 52R + VRHP) / SUMRP	PKP2[2:0] = ”111”	
KVP25	VLCD63 - ΔV x (VRP0 + 68R + VRHP) / SUMRP	PKP3[2:0] = ”000”	VINP4
KVP26	VLCD63 - ΔV x (VRP0 + 69R + VRHP) / SUMRP	PKP3[2:0] = ”001”	
KVP27	VLCD63 - ΔV x (VRP0 + 70R + VRHP) / SUMRP	PKP3[2:0] = ”010”	
KVP28	VLCD63 - ΔV x (VRP0 + 71R + VRHP) / SUMRP	PKP3[2:0] = ”011”	
KVP29	VLCD63 - ΔV x (VRP0 + 72R + VRHP) / SUMRP	PKP3[2:0] = ”100”	
KVP30	VLCD63 - ΔV x (VRP0 + 73R + VRHP) / SUMRP	PKP3[2:0] = ”101”	
KVP31	VLCD63 - ΔV x (VRP0 + 74R + VRHP) / SUMRP	PKP3[2:0] = ”110”	
KVP32	VLCD63 - ΔV x (VRP0 + 75R + VRHP) / SUMRP	PKP3[2:0] = ”111”	
KVP33	VLCD63 - ΔV x (VRP0 + 80R + VRHP) / SUMRP	PKP4[2:0] = ”000”	VINP5
KVP34	VLCD63 - ΔV x (VRP0 + 81R + VRHP) / SUMRP	PKP4[2:0] = ”001”	
KVP35	VLCD63 - ΔV x (VRP0 + 82R + VRHP) / SUMRP	PKP4[2:0] = ”010”	
KVP36	VLCD63 - ΔV x (VRP0 + 83R + VRHP) / SUMRP	PKP4[2:0] = ”011”	
KVP37	VLCD63 - ΔV x (VRP0 + 84R + VRHP) / SUMRP	PKP4[2:0] = ”100”	
KVP38	VLCD63 - ΔV x (VRP0 + 85R + VRHP) / SUMRP	PKP4[2:0] = ”101”	
KVP39	VLCD63 - ΔV x (VRP0 + 86R + VRHP) / SUMRP	PKP4[2:0] = ”110”	
KVP40	VLCD63 - ΔV x (VRP0 + 87R + VRHP) / SUMRP	PKP4[2:0] = ”111”	
KVP41	VLCD63 - ΔV x (VRP0 + 87R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”000”	VINP6
KVP42	VLCD63 - ΔV x (VRP0 + 91R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”001”	
KVP43	VLCD63 - ΔV x (VRP0 + 95R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”010”	
KVP44	VLCD63 - ΔV x (VRP0 + 99R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”011”	
KVP45	VLCD63 - ΔV x (VRP0 + 103R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”100”	
KVP46	VLCD63 - ΔV x (VRP0 + 107R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”101”	
KVP47	VLCD63 - ΔV x (VRP0 + 111R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”110”	
KVP48	VLCD63 - ΔV x (VRP0 + 115R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”111”	
KVP49	VLCD63 - ΔV x (VRP0 + 120R + VRHP + VRLP) / SUMRP	-	VINP7

Table 11. 6 Reference voltages of positive polarity

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0 + VRP1
ΔV: Voltage difference between VLCD63 and of EXVR.

Reference	Formula	Micro-adjusting register	Reference voltage
KVN0	VLCD63 - ΔV x VRN0 / SUMRN	-	VINN0
KVN1	VLCD63 - ΔV x (VRN0 + 5R) / SUMRN	PKN0[2:0] = ”000”	VINN1
KVN2	VLCD63 - ΔV x (VRN0 + 9R) / SUMRN	PKN0[2:0] = ”001”	
KVN3	VLCD63 - ΔV x (VRN0 + 13R) / SUMRN	PKN0[2:0] = ”010”	
KVN4	VLCD63 - ΔV x (VRN0 + 17R) / SUMRN	PKN0[2:0] = ”011”	
KVN5	VLCD63 - ΔV x (VRN0 + 21R) / SUMRN	PKN0[2:0] = ”100”	
KVN6	VLCD63 - ΔV x (VRN0 + 25R) / SUMRN	PKN0[2:0] = ”101”	
KVN7	VLCD63 - ΔV x (VRN0 + 29R) / SUMRN	PKN0[2:0] = ”110”	
KVN8	VLCD63 - ΔV x (VRN0 + 33R) / SUMRN	PKN0[2:0] = ”111”	
KVN9	VLCD63 - ΔV x (VRN0 + 33R + VRHN) / SUMRN	PKN1[2:0] = ”000”	VINN2
KVN10	VLCD63 - ΔV x (VRN0 + 34R + VRHN) / SUMRN	PKN1[2:0] = ”001”	
KVN11	VLCD63 - ΔV x (VRN0 + 35R + VRHN) / SUMRN	PKN1[2:0] = ”010”	
KVN12	VLCD63 - ΔV x (VRN0 + 36R + VRHN) / SUMRN	PKN1[2:0] = ”011”	
KVN13	VLCD63 - ΔV x (VRN0 + 37R + VRHN) / SUMRN	PKN1[2:0] = ”100”	
KVN14	VLCD63 - ΔV x (VRN0 + 38R + VRHN) / SUMRN	PKN1[2:0] = ”101”	
KVN15	VLCD63 - ΔV x (VRN0 + 39R + VRHN) / SUMRN	PKN1[2:0] = ”110”	
KVN16	VLCD63 - ΔV x (VRN0 + 40R + VRHN) / SUMRN	PKN1[2:0] = ”111”	
KVN17	VLCD63 - ΔV x (VRN0 + 45R + VRHN) / SUMRN	PKN2[2:0] = ”000”	VINN3
KVN18	VLCD63 - ΔV x (VRN0 + 46R + VRHN) / SUMRN	PKN2[2:0] = ”001”	
KVN19	VLCD63 - ΔV x (VRN0 + 47R + VRHN) / SUMRN	PKN2[2:0] = ”010”	
KVN20	VLCD63 - ΔV x (VRN0 + 48R + VRHN) / SUMRN	PKN2[2:0] = ”011”	
KVN21	VLCD63 - ΔV x (VRN0 + 49R + VRHN) / SUMRN	PKN2[2:0] = ”100”	
KVN22	VLCD63 - ΔV x (VRN0 + 50R + VRHN) / SUMRN	PKN2[2:0] = ”101”	
KVN23	VLCD63 - ΔV x (VRN0 + 51R + VRHN) / SUMRN	PKN2[2:0] = ”110”	
KVN24	VLCD63 - ΔV x (VRN0 + 52R + VRHN) / SUMRN	PKN2[2:0] = ”111”	
KVN25	VLCD63 - ΔV x (VRN0 + 68R + VRHN) / SUMRN	PKN3[2:0] = ”000”	VINN4
KVN26	VLCD63 - ΔV x (VRN0 + 69R + VRHN) / SUMRN	PKN3[2:0] = ”001”	
KVN27	VLCD63 - ΔV x (VRN0 + 70R + VRHN) / SUMRN	PKN3[2:0] = ”010”	
KVN28	VLCD63 - ΔV x (VRN0 + 71R + VRHN) / SUMRN	PKN3[2:0] = ”011”	
KVN29	VLCD63 - ΔV x (VRN0 + 72R + VRHN) / SUMRN	PKN3[2:0] = ”100”	
KVN30	VLCD63 - ΔV x (VRN0 + 73R + VRHN) / SUMRN	PKN3[2:0] = ”101”	
KVN31	VLCD63 - ΔV x (VRN0 + 74R + VRHN) / SUMRN	PKN3[2:0] = ”110”	
KVN32	VLCD63 - ΔV x (VRN0 + 75R + VRHN) / SUMRN	PKN3[2:0] = ”111”	
KVN33	VLCD63 - ΔV x (VRN0 + 80R + VRHN) / SUMRN	PKN4[2:0] = ”000”	VINN5
KVN34	VLCD63 - ΔV x (VRN0 + 81R + VRHN) / SUMRN	PKN4[2:0] = ”001”	
KVN35	VLCD63 - ΔV x (VRN0 + 82R + VRHN) / SUMRN	PKN4[2:0] = ”010”	
KVN36	VLCD63 - ΔV x (VRN0 + 83R + VRHN) / SUMRN	PKN4[2:0] = ”011”	
KVN37	VLCD63 - ΔV x (VRN0 + 84R + VRHN) / SUMRN	PKN4[2:0] = ”100”	
KVN38	VLCD63 - ΔV x (VRN0 + 85R + VRHN) / SUMRN	PKN4[2:0] = ”101”	
KVN39	VLCD63 - ΔV x (VRN0 + 86R + VRHN) / SUMRN	PKN4[2:0] = ”110”	
KVN40	VLCD63 - ΔV x (VRN0 + 87R + VRHN) / SUMRN	PKN4[2:0] = ”111”	
KVN41	VLCD63 - ΔV x (VRN0 + 87R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”000”	VINN6
KVN42	VLCD63 - ΔV x (VRN0 + 91R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”001”	
KVN43	VLCD63 - ΔV x (VRN0 + 95R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”010”	
KVN44	VLCD63 - ΔV x (VRN0 + 99R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”011”	
KVN45	VLCD63 - ΔV x (VRN0 + 103R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”100”	
KVN46	VLCD63 - ΔV x (VRN0 + 107R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”101”	
KVN47	VLCD63 - ΔV x (VRN0 + 111R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”110”	
KVN48	VLCD63 - ΔV x (VRN0 + 115R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”111”	
KVN49	VLCD63 - ΔV x (VRN0 + 120R + VRHN + VRLN) / SUMRN	-	VINN7

Table 11. 7 Reference voltages of negative polarity

SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN0 + VRN1
ΔV: Voltage difference between VLCD63 and of EXVR.

12. Maximum Rating

Maximum Ratings (Voltage Referenced to VSS)

Symbol	Parameter	Value	Unit
VDD	Supply Voltage	-0.3 to +2.7	V
VDDIO		-0.3 to +4.0	V
VCI	Input Voltage	VSS - 0.3 to 5.0	V
I	Current Drain Per Pin Excluding VDD and VSS	25	mA
TA	Operating Temperature	-30 to +85	℃
Tstg	Storage Temperature	-65 to +150	℃
Ron	Input Resistance	TBD	Ω

Table 12. 1 Maximum ratings

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VCI and VOUT be constrained to the range VSS < VDDIO ≦VCI < VOUT.
Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO).
Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

13. DC Characteristics

DC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 2.2V, T_A = 25℃)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{DD}	System power supply pins of the logic block	Recommend Operating Voltage Possible Operating Voltage	1.8	-	2.50	V
V_{DDIO}	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.4	-	3.6	V
V_{CI}	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO	-	3.6	V
I_{sleep}	Sleep mode current			50		μA
I_{dp}	Operating mode current	100pF loading at Source output		4.0	6	mA
V_{CIM}	Negative V_{CI} Output Voltage	No panel loading	- VCI	-	-	V
V_{CIX2}	V_{CIX2} primary booster efficiency(1)	No panel loading, ITO for V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	83	90	-	%
V_{GH}	Gate driver High Output Voltage Booster efficiency(2)	No panel loading; 4x booster; ITO for C_{YP}, C_{YN}, V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	84	89.5	-	%
		No panel loading; 5x booster; ITO for C_{YP}, C_{YN}, V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	80	88.5	-	%
		No panel loading; 6x booster; ITO for C_{YP}, C_{YN}, V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	72	80	-	%
V_{GL}	Gate driver Low Output Voltage		- V_{GH}		-5.1	V
V_{COMH}	VCOM High Output Voltage		-	-	5.54	V
V_{COML}	VCOM Low Output Voltage		V_{CIM}+0.5	-	-	V
V_{COMA}	VCOM Amplitude		-	-	6	V
V_{LCD63}	V_{LCD63} Output Voltage		-	-	5.57	V
△V_{LCD63}	Max. Source Voltage Variation		-2	-	2	%
V_{OH1}	Logic High Output Voltage	I out = -100μA	0.9*V_{DDIO}	-	V_{DD}	V
V_{VD}	Source Output Voltage Deviation		-	±20	-	mV
V_{OS}	Source Output Voltage Offset		-	-	±30	mV
V_{OL1}	Logic Low Output Voltage	I out = 100μA	0	-	0.1*V_{DDIO}	V
V_{IH1}	Logic High Input voltage		0.8*V_{DDIO}	-	V_{DDIO}	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*V_{DDIO}	V
I_{OH}	Logic High Output Current Source	V out = VDD – 0.4V	50	-	-	μA
I_{OL}	Logic Low Output Current Drain	V out = 0.4V	-	-	-50	μA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	μA
$I_{IL/I\ IH}$	Logic Input Current		-1	-	1	μA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
R_{SON}	Source drivers output resistance		-	1	-	kΩ
R_{GON}	Gate drivers output resistance		-	500	-	Ω
R_{CON}	VCOM output resistance		-	200	-	Ω

Note 1: V_{CIX2} efficiency = V_{CIX2} / (2 x V_{CI}) x 100%
Note 2: V_{GH} efficiency = V_{GH} / (V_{CI} x n) x 100% (where n = booster factor)

Table 13. 1 DC characteristics

14. AC Characteristics

AC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 2.2V, T_A = 25℃)

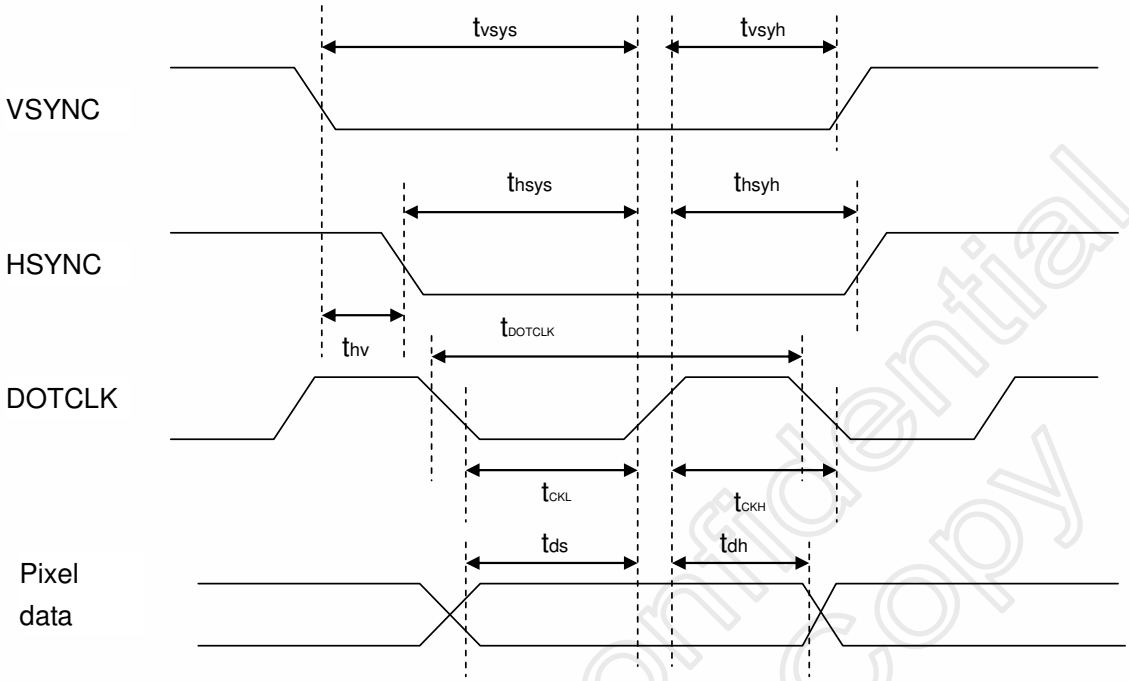


Figure 14. 1 Pixel timing

Characteristics	Symbol	Min		Typ		Max		Unit
		24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency	fDOTCLK	-		6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-		ns
Vertical Sync Setup Time	tvsys	20	10	-		-		ns
Vertical Sync Hold Time	tvsyh	20	10	-		-		ns
Horizontal Sync Setup Time	thsys	20	10	-		-		ns
Horizontal Sync Hold Time	thsyh	20	10	-		-		ns
Phase difference of Sync Signal Falling Edge	thv	1		-		240		tDOTCLK
DOTCLK Low Period	tCKL	50	15	-		-		ns
DOTCLK High Period	tCKH	50	15	-		-		ns
Data Setup Time	tds	12	10	-		-		ns
Data hold Time	tdh	12	10	-		-		ns
Reset pulse width	tRES	10		-		-		us

Note: External clock source must be provided to DOTCLK pin of HX8238-A. The driver will not operate if absent of the clocking signal.

Table 14. 1 Pixel timing

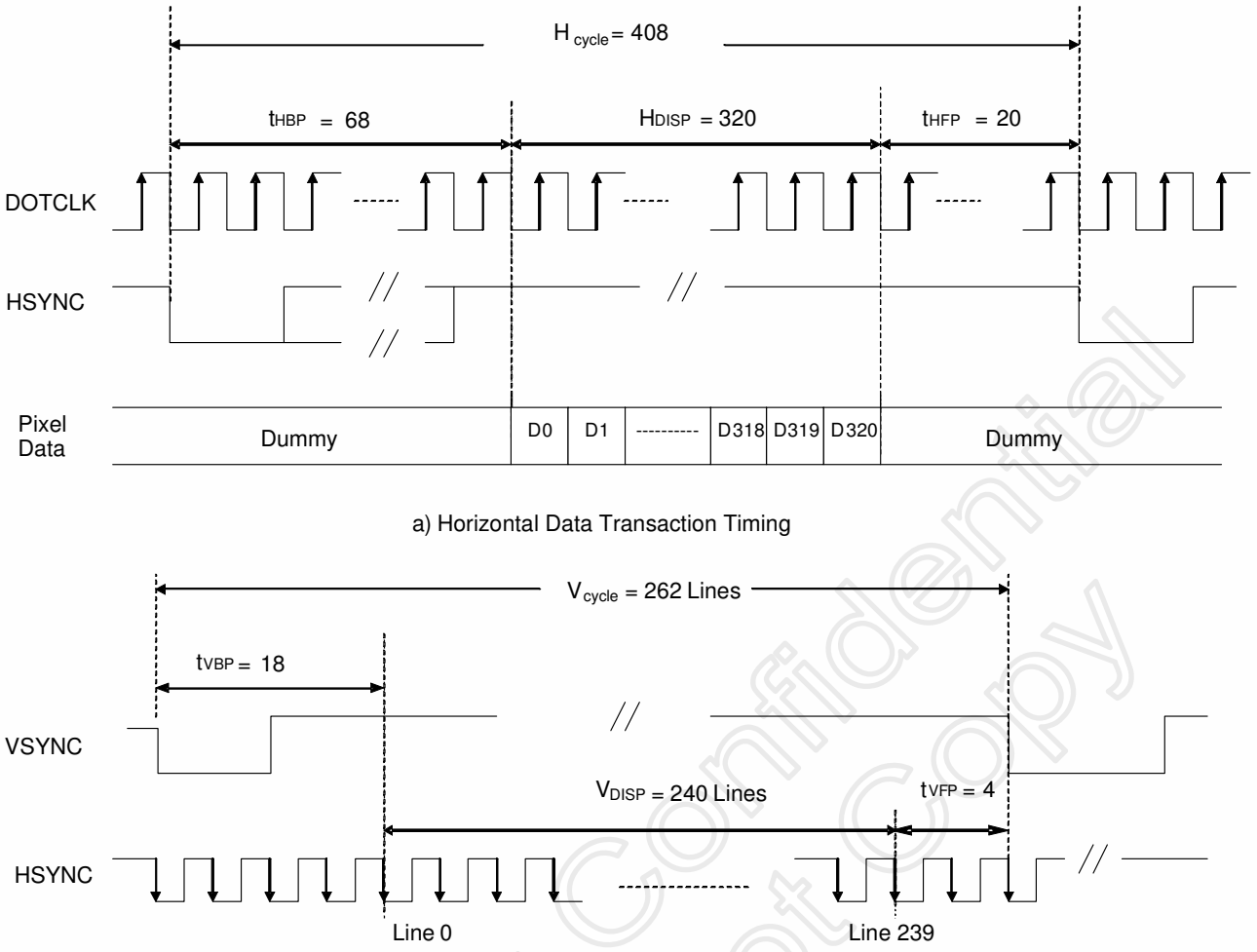


Figure 14. 2 Data transaction timing in parallel RGB (24 bit) interface (SYNC mode)

Characteristics	Symbol	Min		Typ		Max		Unit
		24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency	fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-	-	ns
Horizontal Frequency (Line)	fH	-		14.9		22.35		KHz
Vertical Frequency (Refresh)	fV	-		60		90		Hz
Horizontal Back Porch	tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Front Porch	tHFP	-	-	20	60	-	-	tDOTCLK
Horizontal Data Start Point	tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Blanking Period	tHBP + tHFP	-	-	88	264	-	-	tDOTCLK
Horizontal Display Area	HDISP	-	-	320	960	-	-	tDOTCLK
Horizontal Cycle	Hcycle	-	-	408	1224	450	1350	tDOTCLK
Vertical Back Porch	tVBP	-		18		-		Lines
Vertical Front Porch	tVFP	-		4		-		Lines
Vertical Data Start Point	tVBP	-		18		-		Lines
Vertical Blanking Period	tVBP + tVFP	-		22		-		Lines
Vertical Display Area	VDISP	-		240		-		Lines
Vertical Cycle	Vcycle	-		262		350		Lines

Table 14. 2 Data transaction timing in normal operating mode

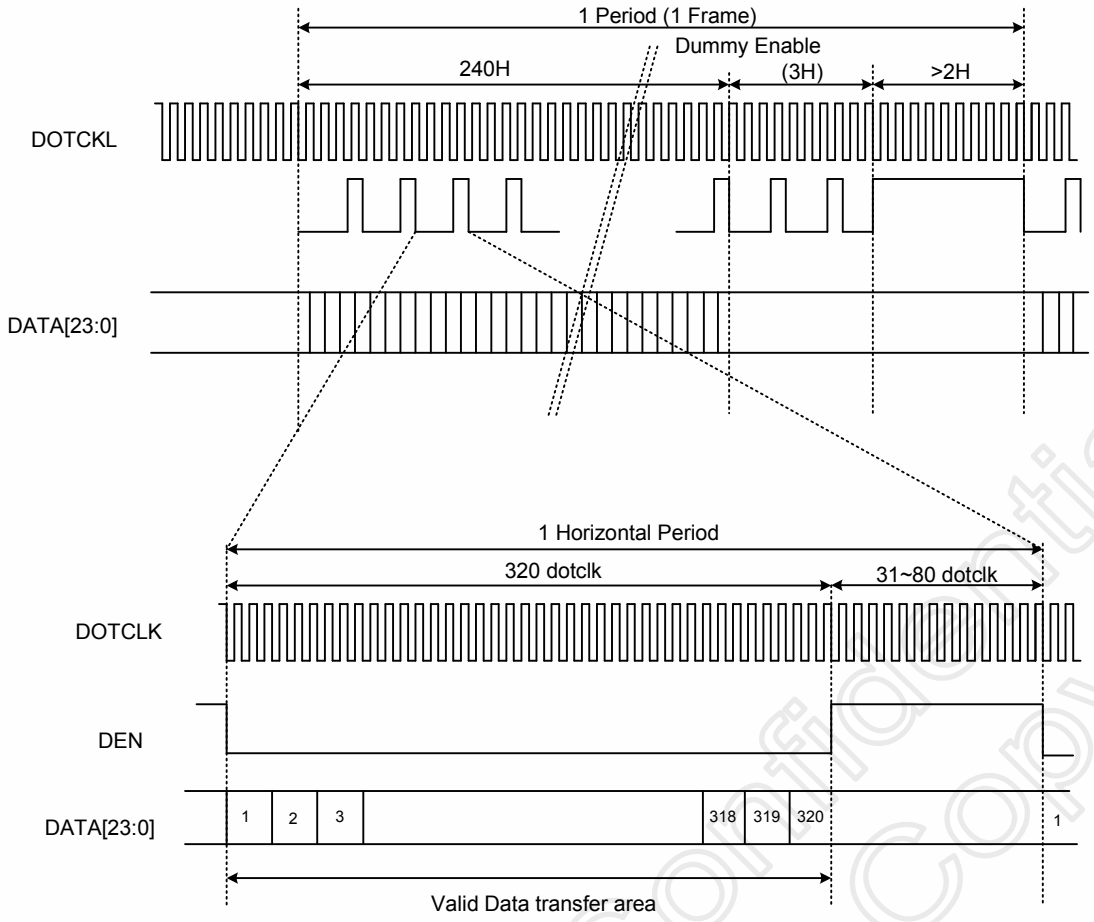
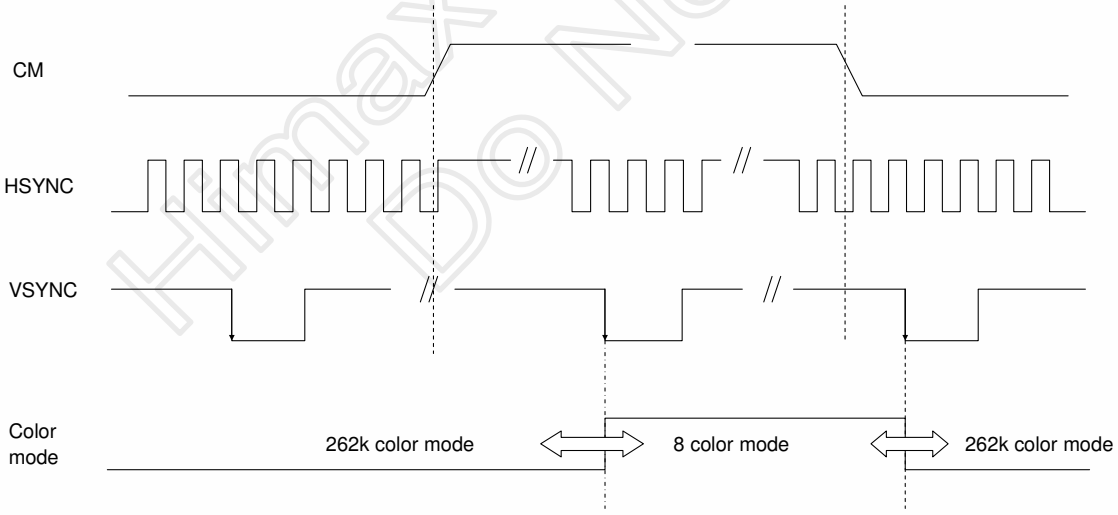


Figure 14. 3 Signal timing in DE mode



Note: The color mode conversion starts at the first falling edge of VSYNC after stage change of CM.

Figure 14. 4 Color mode conversion timing

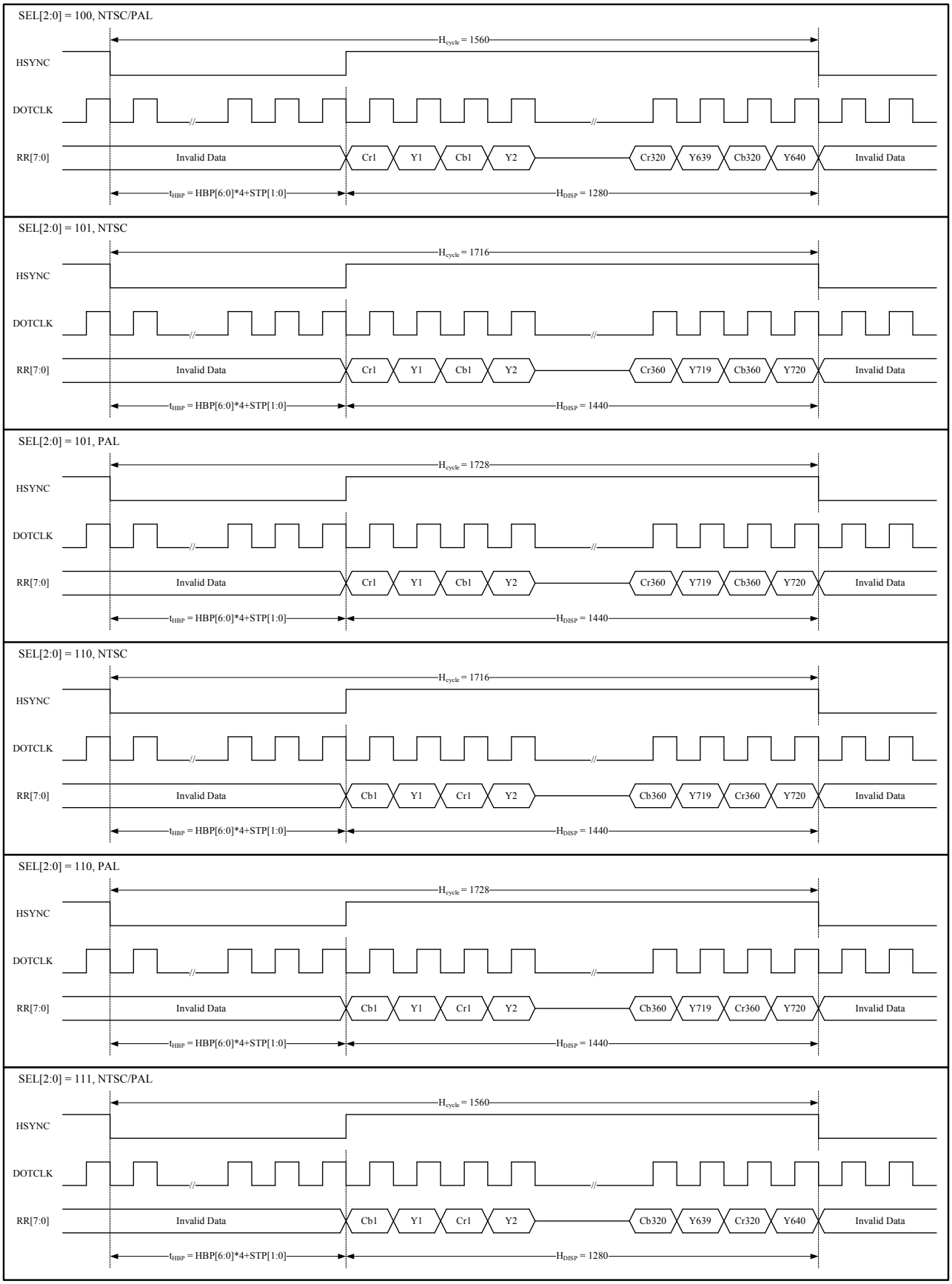


Figure 14. 5 CCIR601 horizontal timing

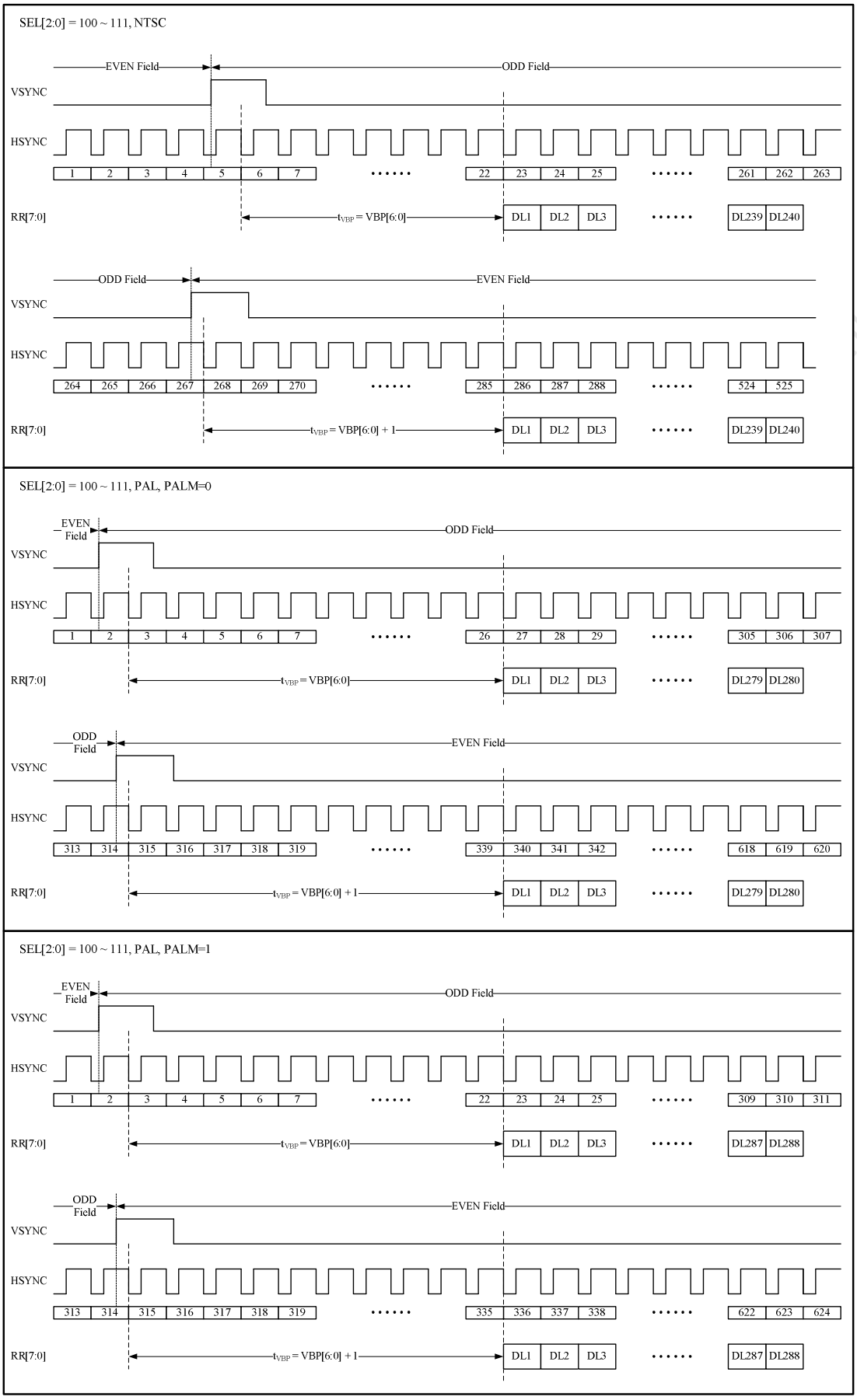


Figure 14. 6 CCIR601 vertical timing

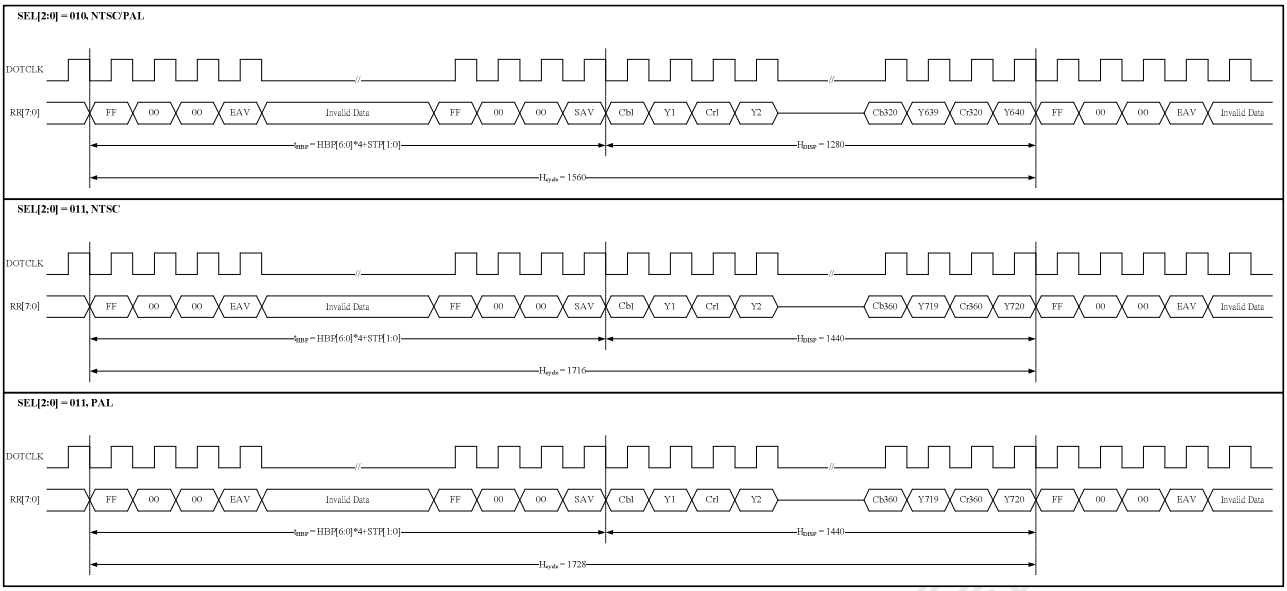


Figure 14. 7 CCIR656 horizontal timing

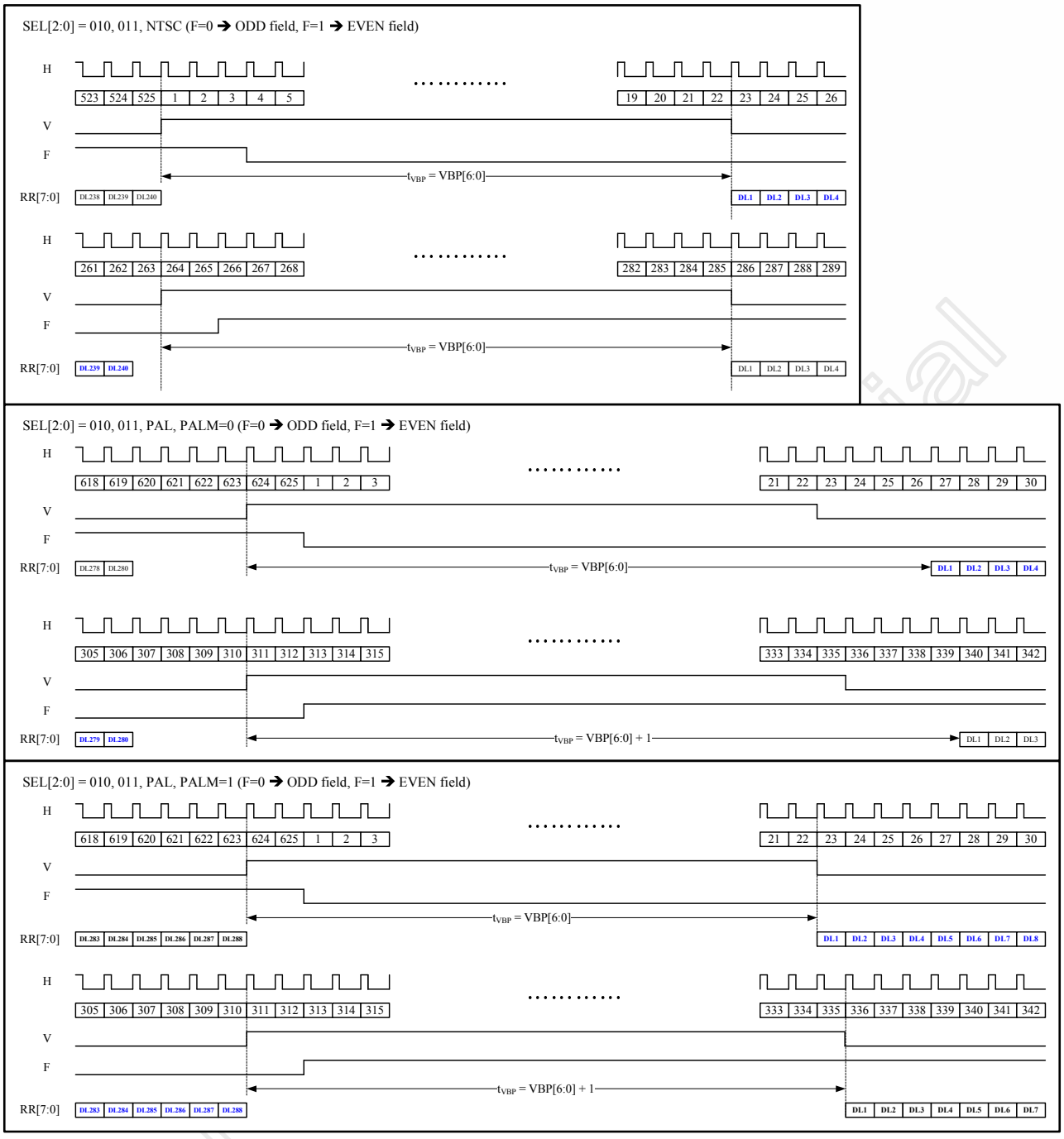


Figure 14. 8 CCIR656 vertical timing

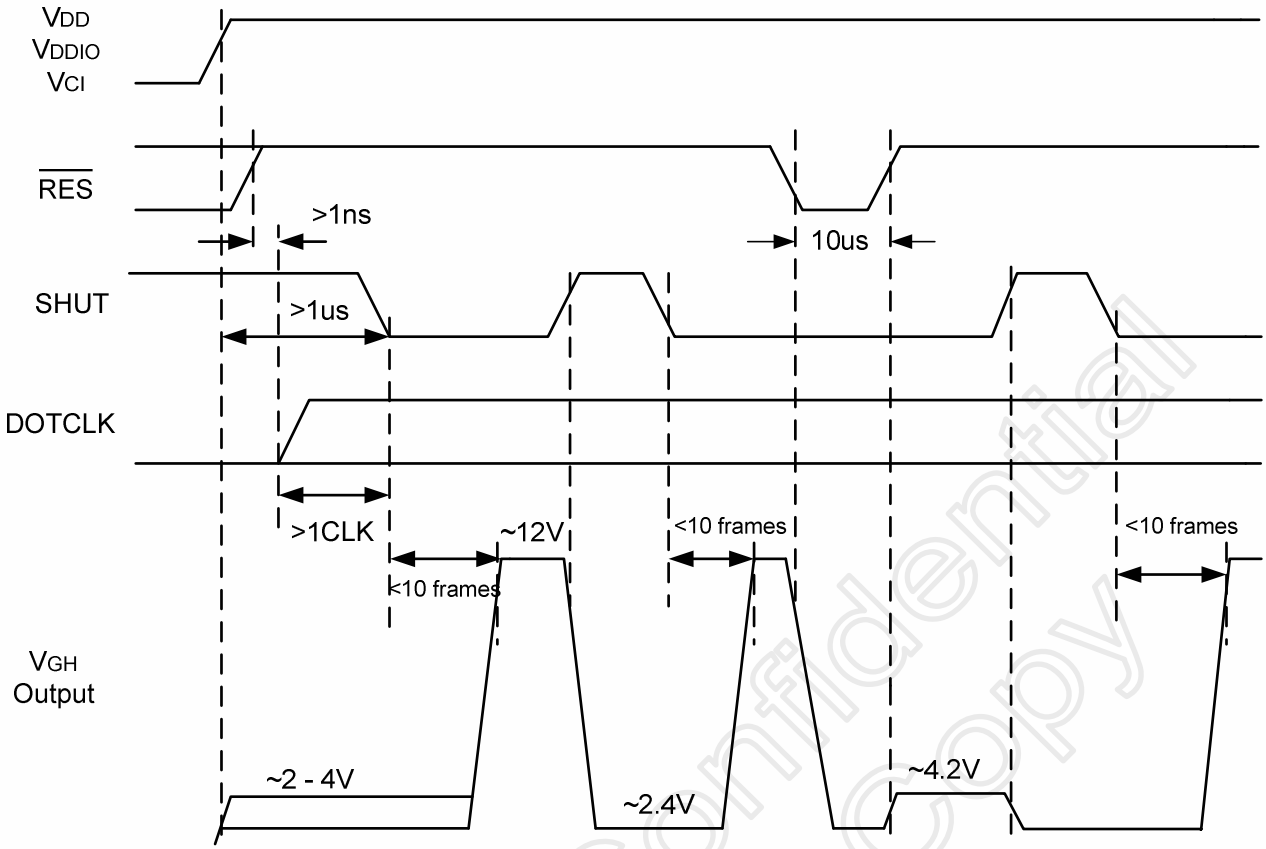


Figure 14. 9 VGH output against SHUT & RES

Note1: The minimum cycle time of SHUT is 10 + 2 frames.
Note2: DOTCLK must be provided for boosting of VGH. The above timing diagram assumed voltages and DOTCLK are continuous supplied after power on.
Note3: VGH and VGL will be forced to VSS at the low stage of RESB.
Note4: The minimum pulse width of RESB is 10us.

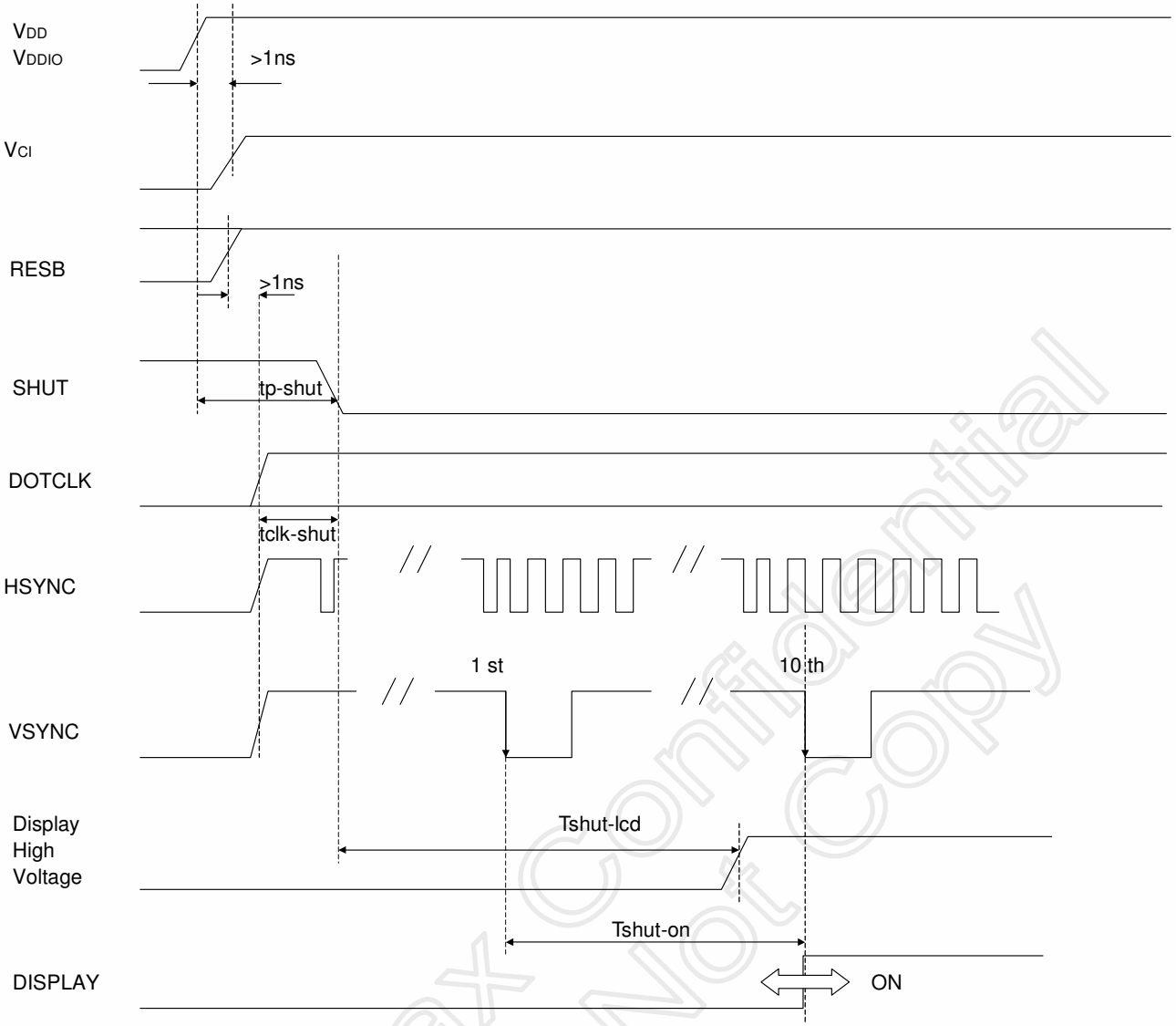


Figure 14. 10 Power up sequence

Characteristics	Symbol	Min	Typ	Max	Units
VDDD / VDDIO on to falling edge of SHUT	tp-shut	1	-	-	us
DOTCLK	tclk-shut	1	-	-	clk
Falling edge of SHUT to LCD power on	tshut-lcd	-	-	128	ms
Falling edge of SHUT to display start - 1 line: 408 clk - 1 frame: 262 line -DOTCLK = 6.5MHz	tshut-on	-	-	10	frame
		-	166	-	ms

Note: It is necessary to input DOTCLK before the falling edge of SHUT.
Display starts at 10th falling edge of VSTNC after the falling edge of SHUT.

Table 14. 3 Power up sequence

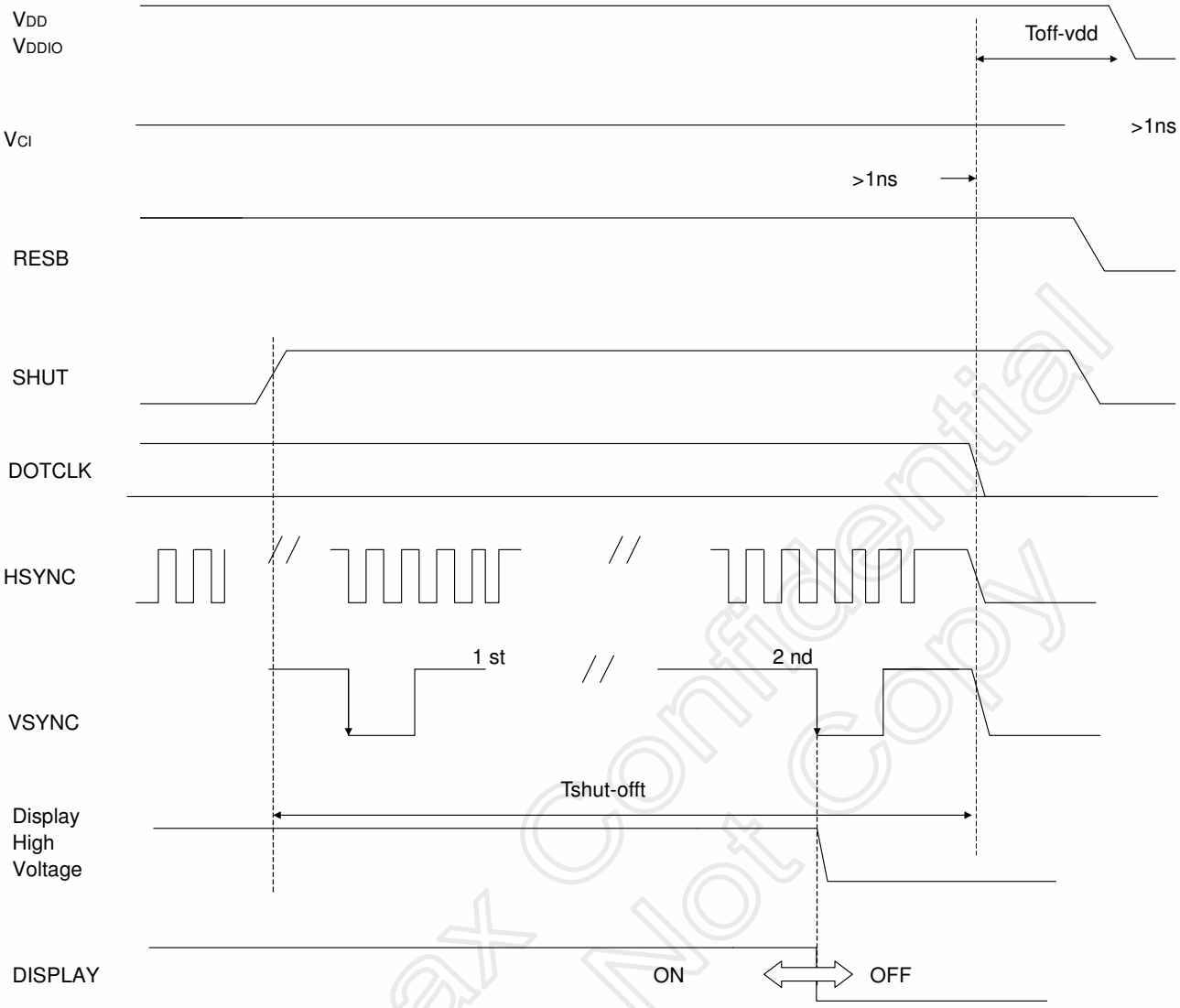
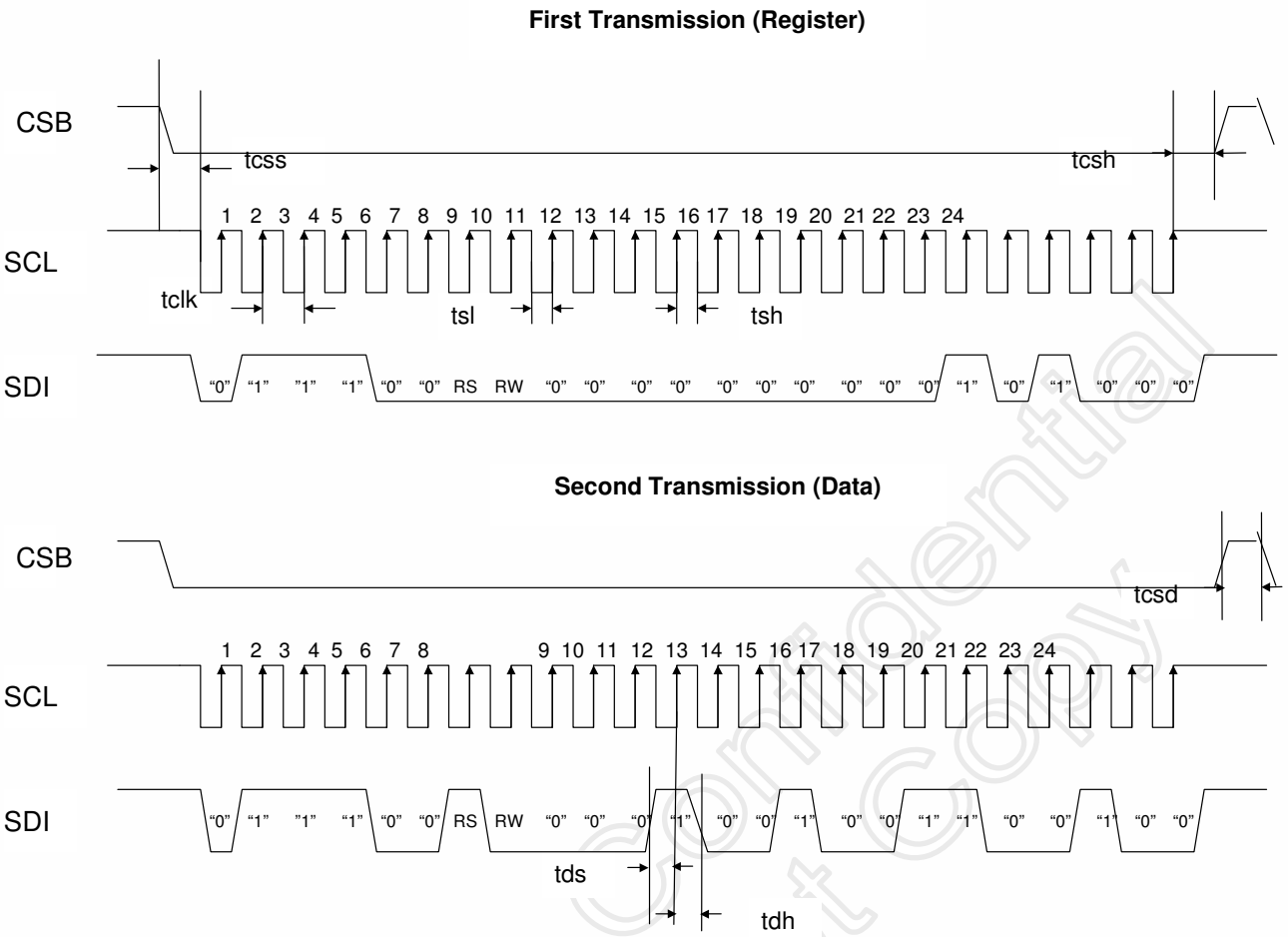


Figure 14. 11 Power down sequence

Characteristics	Symbol	Min	Typ	Max	Uni
Rising edge of SHUT to display off - 1 line: 408 clk - 1 frame: 262 line - DOTCLK = 6.5MHz	tshut-off	2	-	-	frame
		33.4	-	-	ms
Input-signal-off to VDDD / VDDIO off	toff-vdd	1	-	-	us

Note: DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.
Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.
If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

Table 14. 4 Power down sequence



Note: The example transmit "0x1264h" to register R28h.
SPID connected to VSS.

Figure 14. 12 SPI interface timing diagram & transaction example

Characteristics	Symbol	Min	Typ	Max	Unit
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	ns
Clock Low Width	tsl	25	-	-	ns
Clock High Width	tsh	25	-	-	ns
Chip Select Setup Time	tcss	0	-	-	ns
Chip Select Hold Time	tcsh	10	-	-	ns
Chip Select High Delay Time	tcsd	20	-	-	ns
Data Setup Time	tds	5	-	-	ns
Data Hold Time	tdh	10	-	-	ns

Table 14. 5 SPI timing

15. HX8238-A Output Voltage Relationship

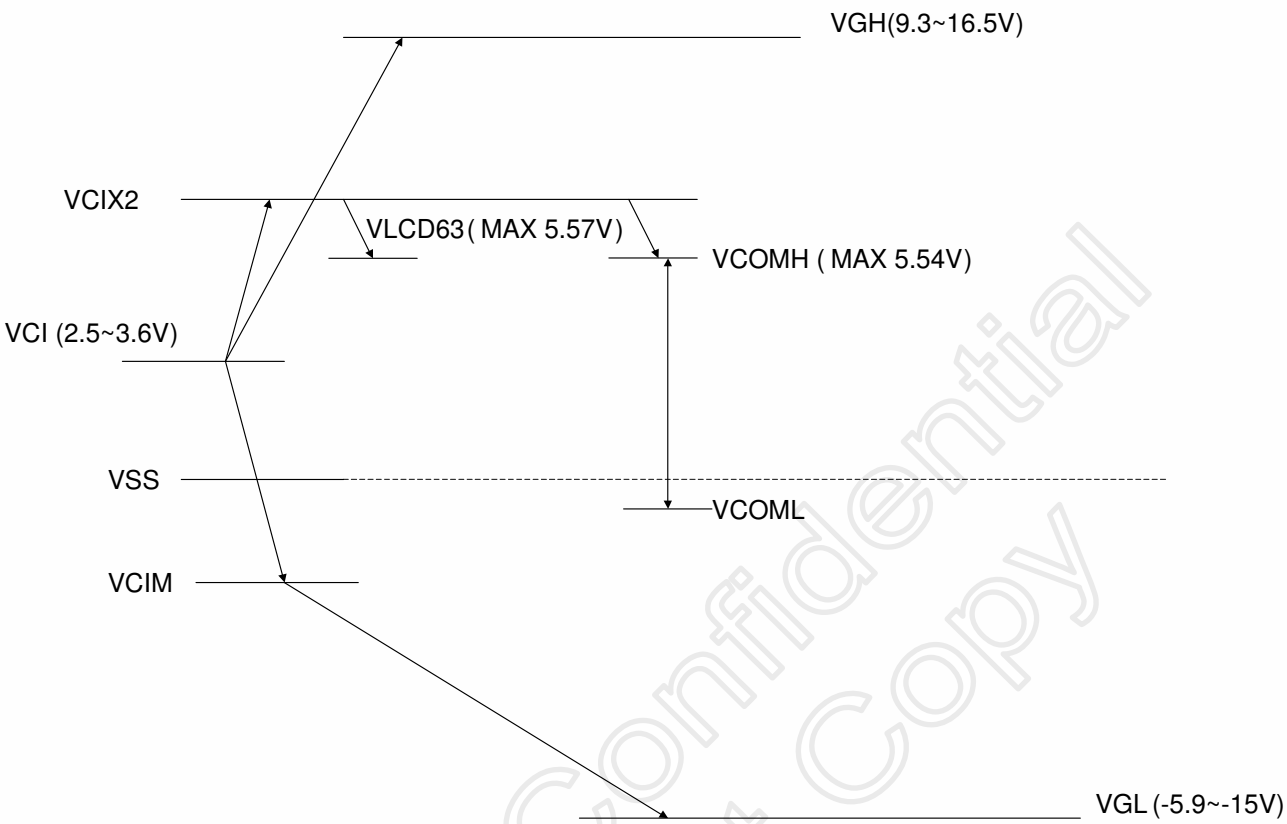


Figure 15. 1 LCD driving voltage relationship

Note: The above voltages level assumed 100% efficiency of the internal booster. There has no voltage drop due to resistance from ITO trace of the panel.

16. Application Circuit

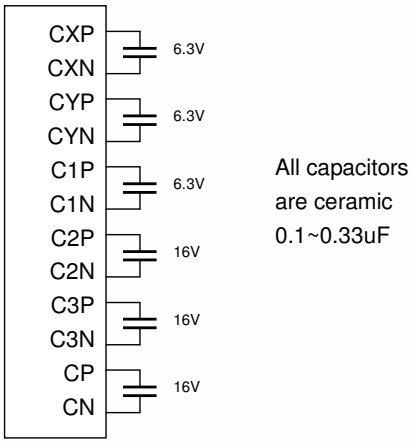


Figure 16. 1 Booster capacitors

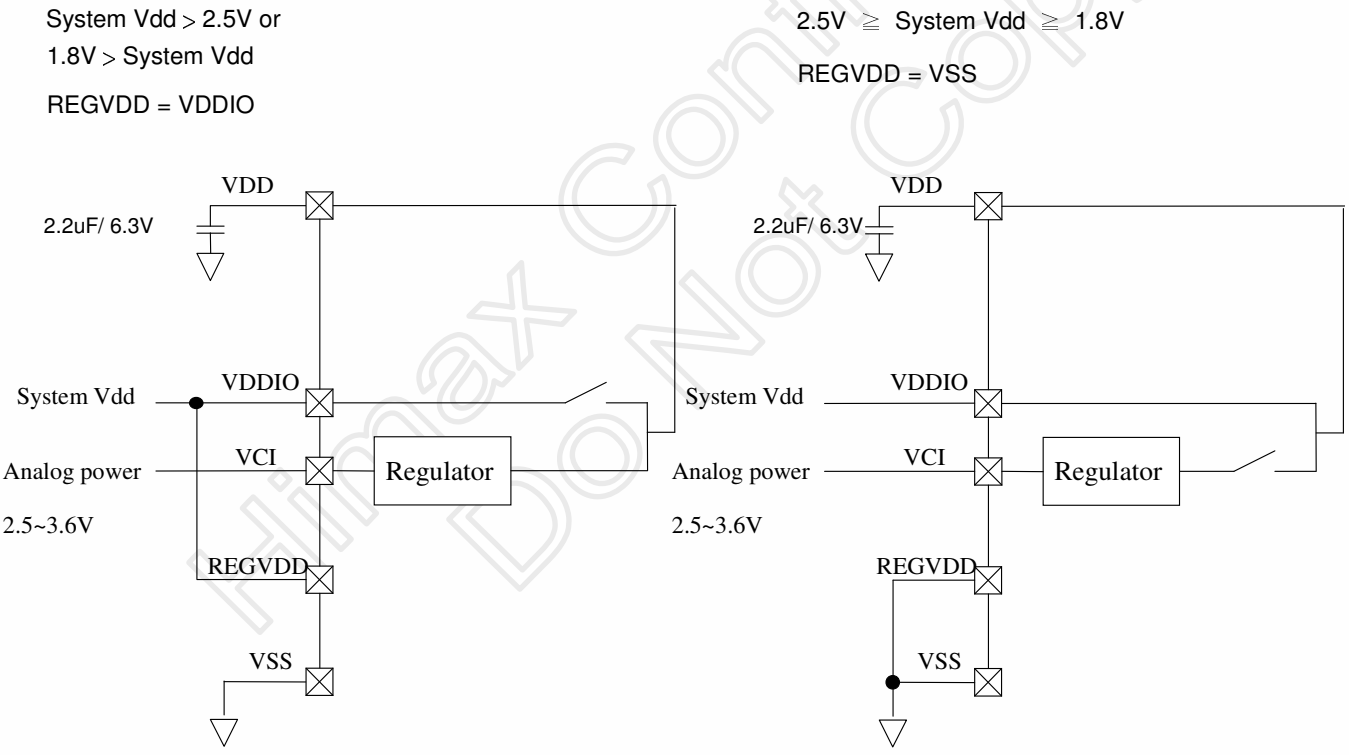


Figure 16. 2 Power supply pins connections

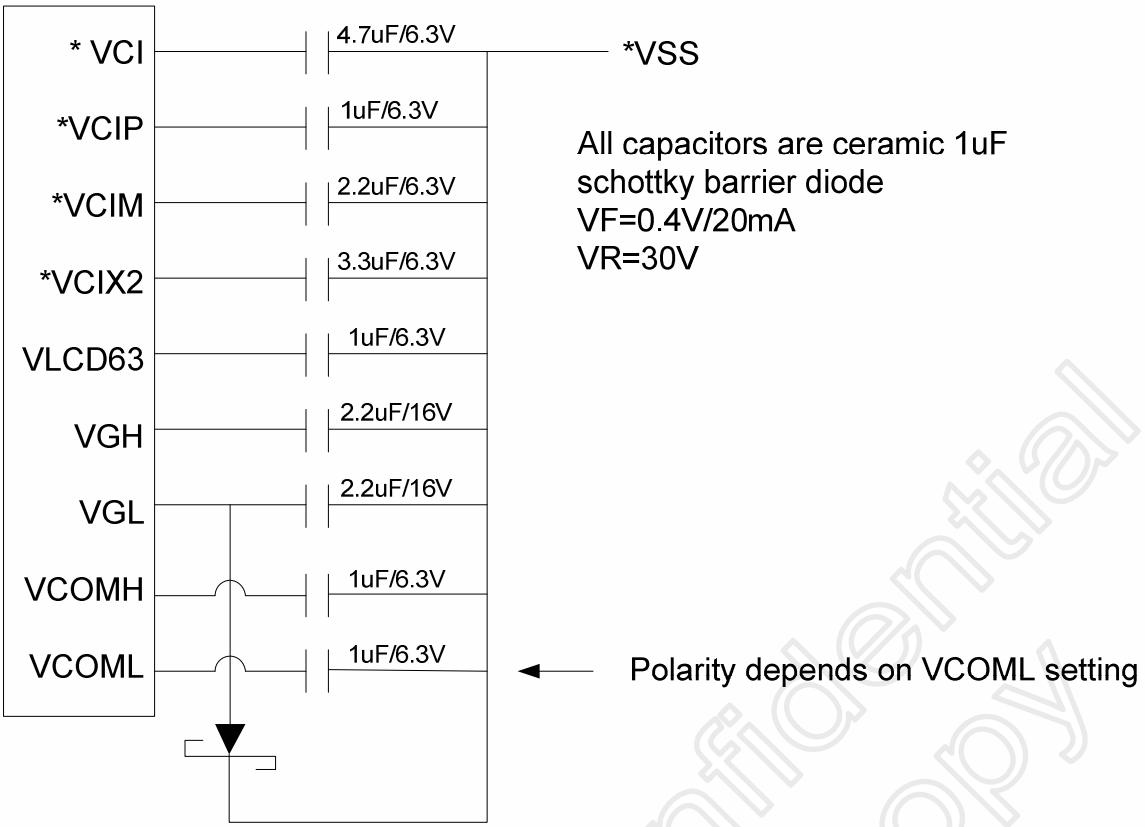


Figure 16. 3 Filtering and charge sharing capacitors

1.Capacitors on VCI should be 4.7uF.
2.Capactiors on VCIP should be 1uF
3.Capacitor on VCIX2 should be 3.3uF
4.Capacitors on VGH, VGL, VCIM should be 2.2uF
5.Other capacitors should be 1uF
* VCIX2 should be separate with VCIX2J at ITO layout to provide noise free path
* VCI should be separate with VCIP at ITO layout to provide noise free path
* VSS should be separate with VCHS, AVSS and VSSRC at ITO layout to provide noise free path

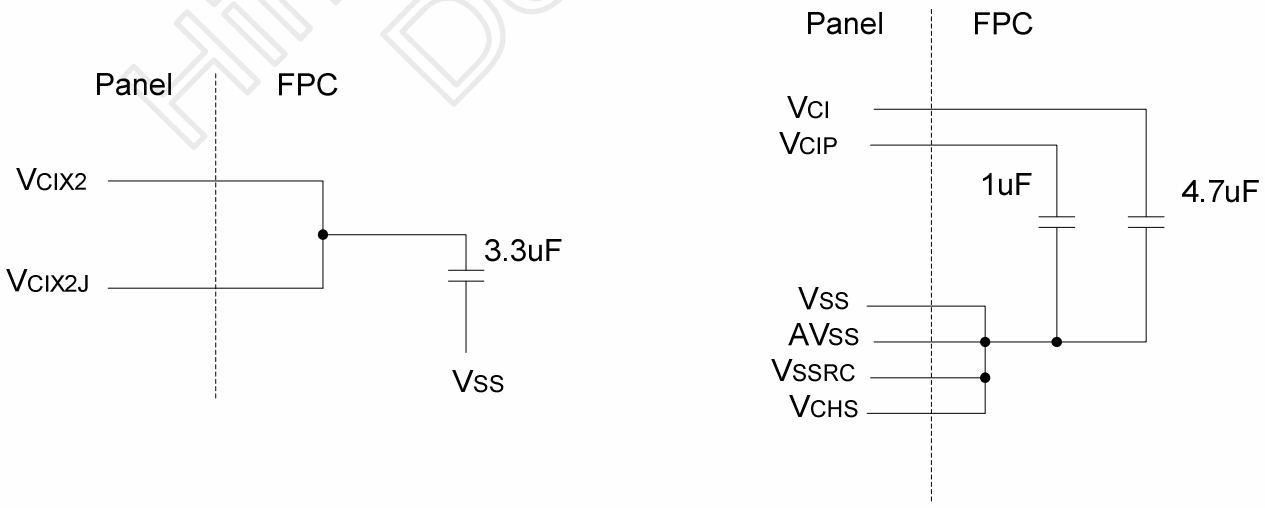


Figure 16. 4 Panel and FPC connection

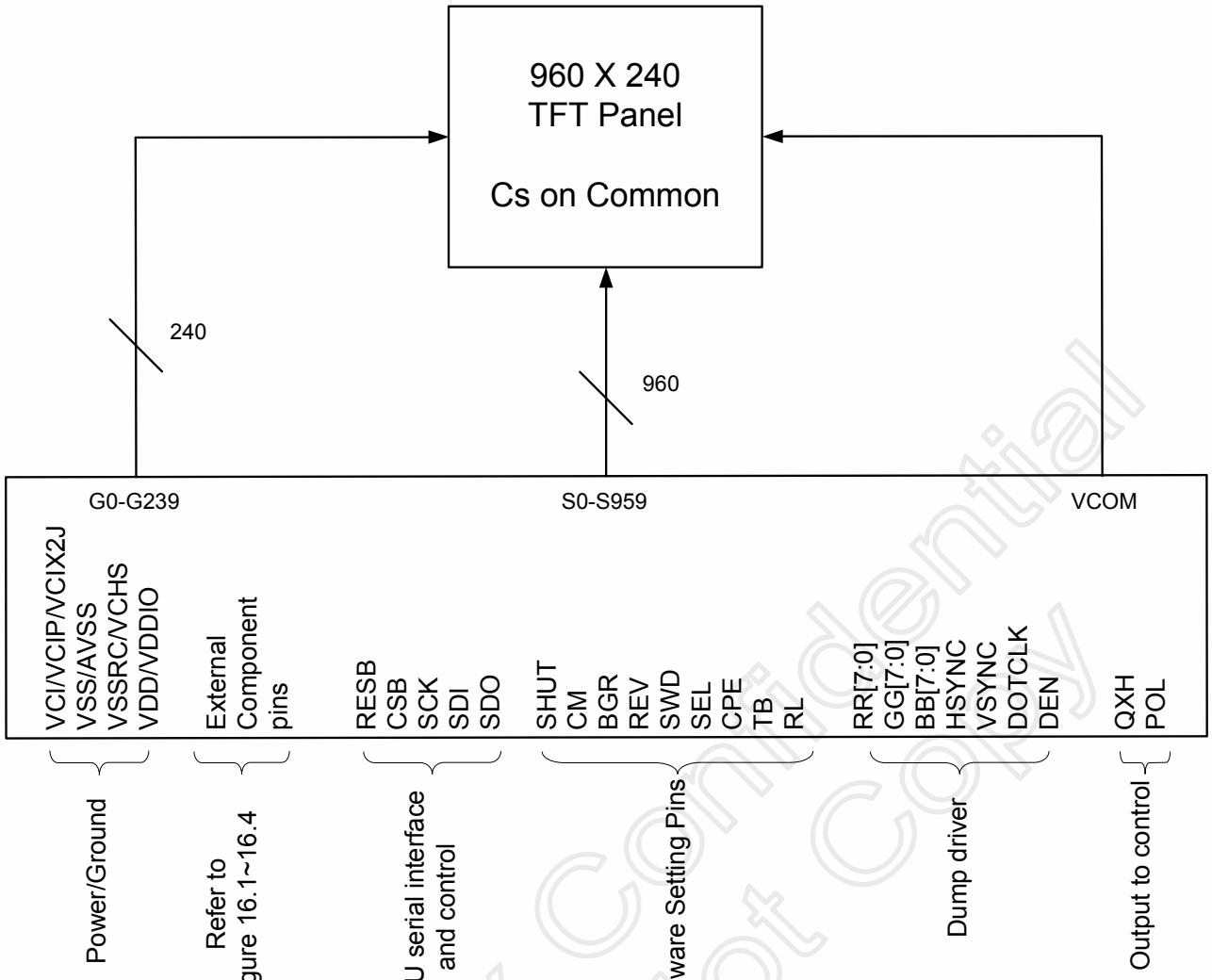


Figure 16.5 Panel connection example

17. Ordering Information

Part NO.	Package
HX8238-A000PDxxx	PD: means COG Xxx: means chip thickness(μm), default 400μm

18. Revision History

Version	EFF.DATE	DESCRIPTION OF CHANGES
00	2006/07/21	New setup
	2006/08/03	1.Change display color to 262K 2.Add register R04h and R05h
	2006/08/16	1. Add POL and QXH pin
	2006/09/08	1.Add PWM function 2.Add Pin Sequence
	2006/09/18	1.Modify pin sequence 2.Add pin SEL[2:0] and SWD[2:0]
	2006/10/11	1.Add CPE pin 2.Add PINV/LPF bits 3.Modify TB pin definition
	2006/10/23	1.Add R0Ah 2.Add GDIS/XDK/GHN bit in R05h 3.Modify pin description for some pull high/low pins 4.Modify gamma table
	2006/10/25	1.Add VDS bit in R0Dh, FB bit in R05h and PALM bit in R04h 2.Update OTP write sequence 3.Add PINV pin 4.Add aging mode 5.Modify data setup/hold time
	2006/11/21	1.Modified the SPI default values. (page 13) 2.Add CCIR601/656 timing. (page 43~46)
01	2006/11/30	1.Add pad location and bump information 2.SWAP C3P/C3N, C2P/C2N, CP/CN, CXP/CXN/CYP/CYN pin sequence 3.Change VDD voltage spec. to 1.8V~2.5V 4.Add VRC[2:0] bit in R0Dh 5.Modify SPI default value
	2007/01/25	1.Modify TEST 4~5 pin definition 2.Modify Figure 4.1 3.Modify Figure 16.2 4.Modify Figure 16.6 5.Modify Figure 16.7 6.Modify Table 9.3 7.Modify Table 9.12 8.Modify Table 14.2